

IPC-2221A

Generic Standard on Printed Board Design

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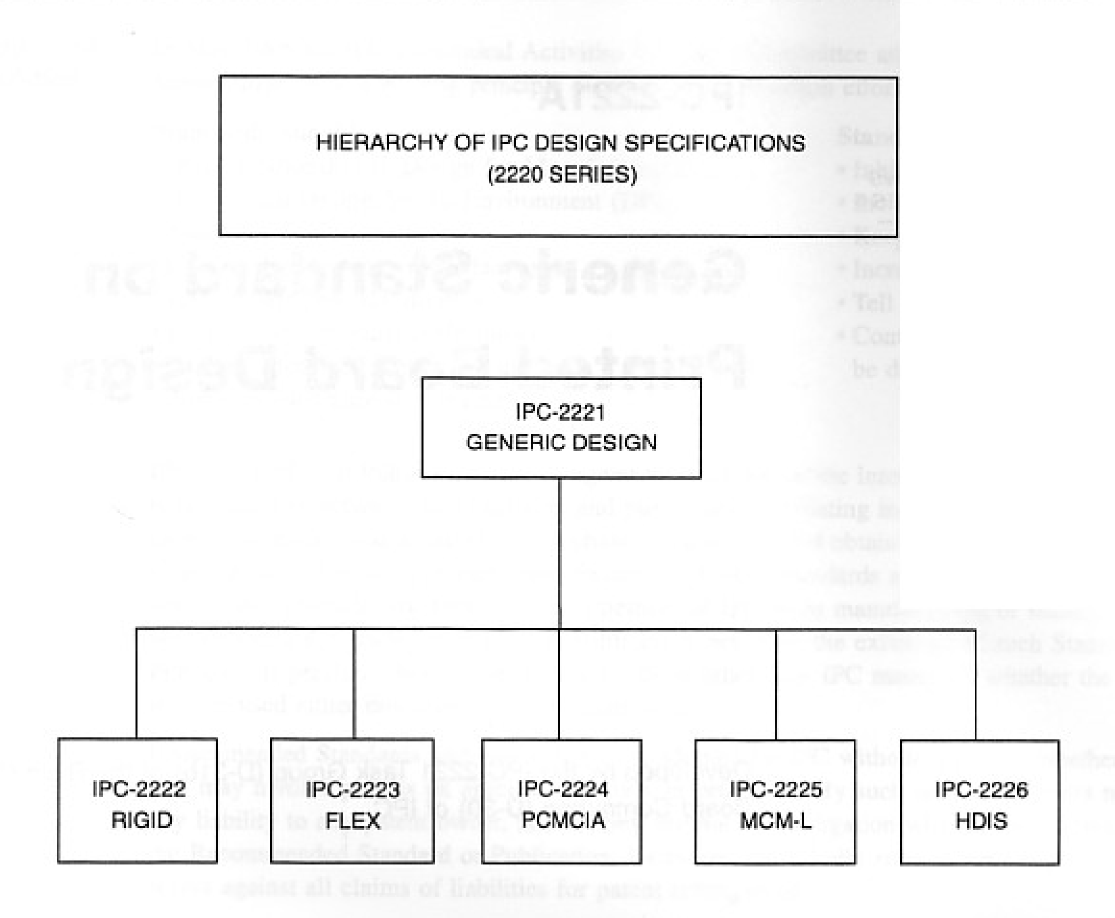
Developed by the IPC-2221 Task Group (D-31b) of the Rigid Printed Board Committee (D-30) of IPC

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Users of this publication are encouraged to participate in the development of future revisions.

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FOREWORD

This standard is intended to provide information on the generic requirements for organic printed board design. All aspects and details of the design requirements are addressed to the extent that they can be applied to the broad spectrum of those designs that use organic materials or organic materials in combination with inorganic materials (metal, glass, ceramic, etc.) to provide the structure for mounting and interconnecting electronic, electromechanical, and mechanical components. It is crucial that a decision pertaining to the choice of product types be made as early as possible. Once a component mounting and interconnecting technology has been selected the user should obtain the sectional document that provides the specific focus on the chosen technology.

It may be more effective to consider alternative printed board construction types for the product being designed. As an example the application of a rigid-flex printed wiring board may be more cost or performance effective than using multiple printed wiring boards, connectors and cables.

IPC's documentation strategy is to provide distinct documents that focus on specific aspect of electronic packaging issues. In this regard document sets are used to provide the total information related to a particular electronic packaging topic. A document set is identified by a four digit number that ends in zero (0).

Included in the set is the generic information which is contained in the first document of the set and identified by the four digit set number. The generic standard is supplemented by one or many sectional documents each of which provide specific focus on one aspect of the topic or the technology selected. The user needs, as a minimum, the generic design document, the sectional of the chosen technology, and the engineering description of the final product.

As technology changes specific focus standards will be updated, or new focus standards added to the document set. The IPC invites input on the effectiveness of the documentation and encourages user response through completion of "Suggestions for Improvement" forms located at the end of each document.

Acknowledgment

Any document involving a complex technology draws material from a vast number of sources. While the principal members of the IPC-2221 Task Group (D-31b) of the Rigid Printed Board Committee (D-30) are shown below, it is not possible to include all of those who assisted in the evolution of this Standard. To each of them, the members of the IPC extend their gratitude.

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Generic Standard on Printed Board Design

1 SCOPE

This standard establishes the generic requirements for the design of organic printed boards and other forms of component mounting or interconnecting structures. The organic materials may be homogeneous, reinforced, or used in combination with inorganic materials; the interconnections may be single, double, or multilayered.

1.1 Purpose The requirements contained herein are intended to establish design principles and recommendations that **shall** be used in conjunction with the detailed requirements of a specific interconnecting structure sectional standard (see 1.2) to produce detailed designs intended to mount and attach passive and active components. This standard is not intended for use as a performance specification for finished boards nor as an acceptance document for electronic assemblies. For acceptability requirements of electronic assemblies, see IPC/EIA-J-STD-001 and IPC-A-610.

The components may be through-hole, surface mount, fine pitch, ultra-fine pitch, array mounting or unpackaged bare die. The materials may be any combination able to perform the physical, thermal, environmental, and electronic function.

1.2 Documentation Hierarchy This standard identifies the generic physical design principles, and is supplemented by various sectional documents that provide details and sharper focus on specific aspects of printed board technology. Examples are:

IPC-2222	Rigid organic printed board structure design
IPC-2223	Flexible printed board structure design
IPC-2224	Organic, PC card format, printed board structure design
IPC-2225	Organic, MCM-L, printed board structure design
IPC-2226	High Density Interconnect (HDI) structure design
IPC-2227	Embedded Passive Devices printed board design (In Process)

The list is a partial summary and is not inherently a part of this generic standard. The documents are a part of the PCB Design Document Set which is identified as IPC-2220. The number IPC-2220 is for ordering purposes only and will include all documents which are a part of the set, whether released or in-process proposal format at the time the order is placed.

1.3 Presentation All dimensions and tolerances in this standard are expressed in hard SI (metric) units and parenthetical soft imperial (inch) units. Users of this and the corresponding performance and qualification specifications are expected to use metric dimensions.

1.4 Interpretation "Shall," the imperative form of the verb, is used throughout this standard whenever a requirement is intended to express a provision that is mandatory. Deviation from a "**shall**" requirement may be considered if sufficient data is supplied to justify the exception.

The words "should" and "may" are used whenever it is necessary to express nonmandatory provisions. "Will" is used to express a declaration of purpose.

To assist the reader, the word "**shall**" is presented in bold characters.

1.5 Definition of Terms The definition of all terms used herein **shall** be as specified in IPC-T-50.

1.6 Classification of Products This standard recognizes that rigid printed boards and printed board assemblies are subject to classifications by intended end item use. Classification of producibility is related to complexity of the design and the precision required to produce the particular printed board or printed board assembly.

Any producibility level or producibility design characteristic may be applied to any end-product equipment category. Therefore, a high-reliability product designated as Class "3" (see 1.6.2), could require level "A" design complexity (preferred producibility) for many of the attributes of the printed board or printed board assembly (see 1.6.3).

1.6.1 Board Type This standard provides design information for different board types. Board types vary per technology and are thus classified in the design sectionals.

1.6.2 Performance Classes Three general end-product classes have been established to reflect progressive increases in sophistication, functional performance requirements and testing/inspection frequency. It should be recognized that there may be an overlap of equipment between classes. The printed board user has the responsibility to determine the class to which his product belongs. The contract **shall** specify the performance class required and indicate any exceptions to specific parameters, where appropriate.

Class 1 General Electronic Products Includes consumer products, some computer and computer peripherals, as well as general military hardware suitable for applications where cosmetic imperfections are not important and the

major requirement is function of the completed printed board or printed board assembly.

Class 2 Dedicated Service Electronic Products Includes communications equipment, sophisticated business machines, instruments and military equipment where high performance and extended life is required, and for which uninterrupted service is desired but is not critical. Certain cosmetic imperfections are allowed.

Class 3 High Reliability Electronic Products Includes the equipment for commercial and military products where continued performance or performance on demand is critical. Equipment downtime cannot be tolerated, and must function when required such as for life support items, or critical weapons systems. Printed boards and printed board assemblies in this class are suitable for applications where high levels of assurance are required and service is essential.

1.6.3 Producibility Level When appropriate this standard will provide three design producibility levels of features, tolerances, measurements, assembly, testing of completion or verification of the manufacturing process that reflect progressive increases in sophistication of tooling, materials or processing and, therefore progressive increases in fabrication cost. These levels are:

Level A General Design Producibility—Preferred
Level B Moderate Design Producibility—Standard
Level C High Design Producibility—Reduced

The producibility levels are not to be interpreted as a design requirement, but a method of communicating the degree of difficulty of a feature between design and fabrication/assembly facilities. The use of one level for a specific feature does not mean that other features must be of the same level. Selection should always be based on the minimum need, while recognizing that the precision, performance, conductive pattern density, equipment, assembly and testing requirements determine the design producibility level. The numbers listed within the numerous tables are to be used as a guide in determining what the level of producibility will be for any feature. The specific requirement for any feature that must be controlled on the end item **shall** be specified on the master drawing of the printed board or the printed board assembly drawing.

1.7 Revision Level Changes Changes made to this revision of the IPC-2221 are indicated throughout by gray-shading of the relevant subsection(s). Changes to a figure or table are indicated by gray-shading of the Figure or Table header.

2 APPLICABLE DOCUMENTS

The following documents form a part of this document to the extent specified herein. If a conflict of requirements exist between IPC-2221 and those listed below, IPC-2221 takes precedence.

2.1 IPC[1]

IPC-A-22 UL Recognition Test Pattern

IPC-A-43 Ten-Layer Multilayer Artwork

IPC-A-47 Composite Test Pattern Ten-Layer Phototool

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-CF-152 Composite Metallic Material Specification for Printed Wiring Boards

IPC-D-279 Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

IPC-D-310 Guidelines for Phototool Generation and Measurement Techniques

IPC-D-317 Design Guidelines for Electronic Packaging Utilizing High-speed Techniques

IPC-D-322 Guidelines for Selecting Printed Wiring Board Sizes Using Standard Panel Sizes

IPC-D-325 Documentation Requirements for Printed Boards

IPC-D-330 Design Guide Manual

IPC-D-356 Bare Substrate Electrical Test Data Format

IPC-D-422 Design Guide for Press Fit Rigid Printed Board Backplanes

IPC-TM-650 Test Methods Manual[2]

Method 2.4.22C 06/99 Bow and Twist

IPC-CM-770 Printed Board Component Mounting

IPC-SM-780 Component Packaging and Interconnecting with Emphasis on Surface Mounting

IPC-SM-782 Surface Mount Design and Land Pattern Standard

IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments

IPC-MC-790 Guidelines for Multichip Module Technology Utilization

1. www.ipc.org
2. Current and revised IPC Test Methods are available through IPC-TM-650 subscription and on the IPC Web site (www.ipc.org/html/testmethods.htm).

IPC-CC-830 Qualification and Performance of Electrical Insulating Compound for Printed Board

IPC-SM-840 Qualification and Performance of Permanent Polymer Coating (Solder Mask) for Printed Boards

IPC-2141 Controlled Impedance Circuit Boards and High Speed Logic Design

IPC-2511 Generic Requirements for Implementation of Product Manufacturing Description Data and Transfer Methodology

IPC-2513 Drawing Methods for Manufacturing Data Description

IPC-2514 Printed Board Manufacturing Data Description

IPC-2515 Bare Board Product Electrical Testing Data Description

IPC-2516 Assembled Board Product Manufacturing

IPC-2518 Parts List Product Data Description

IPC-2615 Printed Board Dimensions and Tolerances

IPC-4101 Specification for Base Materials for Rigid and Multilayer Printed Boards

IPC-4202 Flexible Base Dielectrics for Use in Flexible Printed Circuitry

IPC-4203 Adhesive Coated Dielectric Films for Use as Cover Sheets for Flexible Printed Wiring and Flexible Bonding Films

IPC-4204 Flexible Metal-Clad Dielectrics for Use in Fabrication of Flexible Printed Circuitry

IPC-4552 Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Circuit Boards

IPC-4562 Metal Foil for Printed Wiring Applications

IPC-6011 Generic Performance Specification for Printed Boards

IPC-6012 Qualification and Performance Specification for Rigid Printed Boards

IPC-7095 Design and Assembly Process Implementation for BGAs

IPC-9701 Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments

IPC-9252 Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards

SMC-TR-001 An Introduction to Tape Automated Bonding Fine Pitch Technology

2.2 Joint Industry Standards[3]

J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

J-STD-003 Solderability Tests for Printed Boards

J-STD-005 Requirements for Soldering Pastes

J-STD-006 Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications

J-STD-012 Implementation of Flip Chip and Chip Scale Technology

J-STD-013 Implementation of Ball Grid Array and Other High Density Technology

2.3 Society of Automotive Engineers[4]

SAE-AMS-QQ-A-250 Aluminum Alloy, Plate and Sheet

SAE-AMS-QQ-N-290 Nickel Plating (Electrodeposited)

2.4 American Society for Testing and Materials[5]

ASTM-B-152 Copper Sheet, Strip and Rolled Bar

ASTM-B-488 Standard Specification for Electrodeposited Coatings of Gold for Engineering Use

ASTM-B-579 Standard Specification for Electrodeposited Coating of Tin-Lead Alloy (Solder Plate)

2.5 Underwriters Labs[6]

UL-746E Standard Polymeric Materials, Material used in Printed Wiring Boards

2.6 IEEE[7]

IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture

3. www.ipc.org
4. www.sae.org
5. www.astm.org
6. www.ul.com
7. www.ieee.org

2.7 ANSI[8]

ANSI/EIA 471 Symbol and Label for Electrostatic Sensitive Devices

3 GENERAL REQUIREMENTS

The information contained in this section describes the general parameters to be considered by all disciplines prior to and during the design cycle.

Designing the physical features and selecting the materials for a printed wiring board involves balancing the electrical, mechanical and thermal performance as well as the reliability, manufacturing and cost of the board. The tradeoff checklist (see Table 3-1) identifies the probable effect of changing each of the physical features or materials. The items in the checklist need to be considered if it is necessary to change a physical feature or material from one of the established rules. Cost can also be affected by these parameters as well as those in Table 5-1.

How to read Table 3-1: As an example, the first row of the table indicates that if the dielectric thickness to ground is increased, the lateral crosstalk also increases and the resultant performance of the PCB is degraded (because lateral crosstalk is not a desired property).

Table 3-1 PCB Design/Performance Tradeoff Checklist

Design Feature	Class Electrical Performance (EP) Mechanical Performance (MP) Reliability (R) Manufacturability/ Yield (M/Y)	Performance Parameter	Impact if Design Feature is Increased			
			Performance Parameter is:		Resulting Performance or Reliability is:	
			Increased	Decreased	Enhanced	Degraded
Dielectric Thickness to Ground	EP	Lateral Crosstalk	X			X
	EP	Vertical Crosstalk	X			X
	EP	Characteristic Impedance	X		Design Driven	
	MP	Physical Size/Weight	X			X
Line Spacing	EP	Lateral Crosstalk		X	X	
	EP	Vertical Crosstalk		X	X	
	MP	Physical Size/Weight	X			X
	M/Y	Electrical Isolation	X		X	
Coupled Line Length	EP	Lateral Crosstalk	X			X
	EP	Vertical Crosstalk	X			X
Line Width	EP	Lateral Crosstalk		X	X	
	EP	Vertical Crosstalk	X			X
	EP	Characteristic Impedance		X	Design Driven	
	MP	Physical Size/Weight	X		Design Driven	
	R	Signal Conductor Integrity	X		X	
	M/Y	Electrical Continuity	X		X	
Line Thickness	EP	Lateral Crosstalk	X			X
	R	Signal Conductor Integrity	X		X	
Vertical Line Spacing	EP	Vertical Crosstalk		X	X	
Z_o of PCB vs. Z_o of Device	EP	Reflections		X	X	
Distance between Via Walls	R	Electrical Isolation	X		X	
Annular Ring (capture and target land to via)	M/Y	Producibility	X		X	
Signal Layer Quantity	MP	Physical Size/Weight	X			X
	M/Y	Layer-to-Layer Registration		X		X

8. www.ansi.org

Design Feature	Class Electrical Performance (EP) Mechanical Performance (MP) Reliability (R) Manufacturability/ Yield (M/Y)	Performance Parameter	Impact if Design Feature is Increased			
			Performance Parameter is:		Resulting Performance or Reliability is:	
			Increased	Decreased	Enhanced	Degraded
Component I/O Pitch Board Thickness	MP	Physical Size/Weight	X			X
	R	Via Integrity		X		X
	M/Y	Via Plating Thickness		X		X
Copper Plating Thickness	R	Via Integrity	X		X	
Aspect Ratio	R	Via Integrity		X		X
	M/Y	Producibility		X		X
Overplate (Nickel -Kevlar only)	R	Via Integrity	X		X	
Via Diameter	M/Y	Via Plating Thickness	X		X	
	R	Via Integrity	X		X	
Laminate Thickness (Core)	EP	Lateral Crosstalk	X			X
	EP	Vertical Crosstalk		X	X	
	EP	Characteristic Impedance	X		Design Driven	
	MP	Physical Size/Weight	X			X
	R	Via Integrity		X		X
	MP	Flatness Stability	X		X	
Prepreg Thickness (Core)	EP	Lateral Crosstalk	X			X
	EP	Vertical Crosstalk		X	X	
	EP	Characteristic Impedance	X		Design Driven	
	EP	Physical Size/Weight	X			X
	R	Via Integrity		X		X
Dielectric Constant	EP	Reflections	X			X
	EP	Characteristic Impedance		X	Design Driven	
	EP	Signal Speed		X	Design Driven	
CTE (out-of-plane)	R	Via Integrity		X		X
CTE (in-plane)	R	Solder Joint Integrity		X		X
	R	Signal Conductor Integrity		X		X
Resin T_g	R	Via Integrity	X		X	
	R	PTH Solder Joint Integrity	X		X	
Copper Ductility	R	Via Integrity	X		X	
	R	Signal Conductor Integrity	X		X	
Copper Peel Strength	R	Component Land Adhesion to Dielectric	X		X	
Dimensional Stability	M/Y	Layer-to-Layer Registration	X		X	
Resin Flow	M/Y	PWB Resin Voids		X	X	
Rigidity	MP	Flexural Modulus	X		Design Driven	
Volatile Content	M/Y	PWB Resin Voids	X			X

3.1 Information Hierarchy

3.1.1 Order of Precedence In the event of any conflict in the development of new designs, the following order of precedence **shall** prevail:

1. The procurement contract.
2. The master drawing or assembly drawing (supplemented by an approved deviation list, if applicable).
3. This standard.
4. Other applicable documents.

3.2 Design Layout The layout generation process should include a formal design review of layout details by as many affected disciplines within the company as possible, including fabrication, assembly and testing. The approval of the layout by representatives of the affected disciplines will ensure that these production-related factors have been considered in the design.

The success or failure of an interconnecting structure design depends on many interrelated considerations. From an end-product usage standpoint, the impact on the design by the following typical parameters should be considered.

- Equipment environmental conditions, such as ambient temperature, heat generated by the components, ventilation, shock and vibration.
- If an assembly is to be maintainable and repairable, consideration must be given to component/circuit density, the selection of board/conformal coating materials, and component placement for accessibility.
- Installation interface that may affect the size and location of mounting holes, connector locations, lead protrusion limitations, part placement, and the placement of brackets and other hardware.
- Testing/fault location requirements that might affect component placement, conductor routing, connector contact assignments, etc.
- Process allowances such as etch factor compensation for conductor widths, spacings, land fabrication, etc. (see Section 5 and Section 9).
- Manufacturing limitations such as minimum etched features, minimum plating thickness, board shape and size, etc.
- Coating and marking requirements.
- Assembly technology used, such as surface mount, through hole, and mixed.
- Board performance class (see 1.6.2).
- Materials selection (see Section 4).
- Producibility of the printed board assembly as it pertains to manufacturing equipment limitations.
  –Flexibility (Flexural) Requirements
  –Electrical/Electronic
  –Performance Requirements
- ESD sensitivity considerations.

3.2.1 End-Product Requirements The end-product requirements **shall** be known prior to design start-up. Maintenance and serviceability requirements are important factors which need to be addressed during the design phase. Frequently, these factors affect layout and conductor routing.

3.2.2 Density Evaluation A wide variety of materials and processes have been used to create substrates for electronics over the last half century, from traditional printed circuits made from resins (i.e., epoxy), reinforcements (i.e., glass cloth or paper), and metal foil (i.e., copper), to ceramics metallized by various thin and thick film techniques. However, they all share a common attribute; they must route signals through conductors.

There are also limits to how much routing each can accommodate. The factors that define the limits of their wire routing ability as a substrate are:

- Pitch/distance between vias or holes in the substrate.
- Number of wires that can be routed between those vias.
- Number of signal layers required.

In addition, the methods of producing blind and buried vias can facilitate routing by selectively occupying routing channels. Vias that are routed completely through the printed board preclude any use of that space for routing on all conductor layers.

These factors can be combined to create an equation that defines the wire routing ability of a technology. In the past, most components had terminations along the periphery on two or more sides. However area array components are more space conservative and allow coarser I/O pitches to be used (see Figure 3-1).

3.3 Schematic/Logic Diagram The initial schematic/logic diagram designates the electrical functions and interconnectivity to be provided to the designer for the printed board and its assembly. This schematic should define, when applicable, critical circuit layout areas, shielding requirements, grounding and power distribution requirements, the allocation of test points, and any preassigned input/output connector locations. Schematic information may be generated as hard copy or computer data (manually or automated).

3.4 Parts List A parts list is a tabulation of parts and materials used in the construction of a printed board assembly. All end item identifiable parts and materials **shall** be identified in the parts list or on the field of the drawing. Excluded are those materials used in the manufacturing process, but may include reference information; i.e., specifications pertinent to the manufacture of the assembly and reference to the schematic/logic diagram.

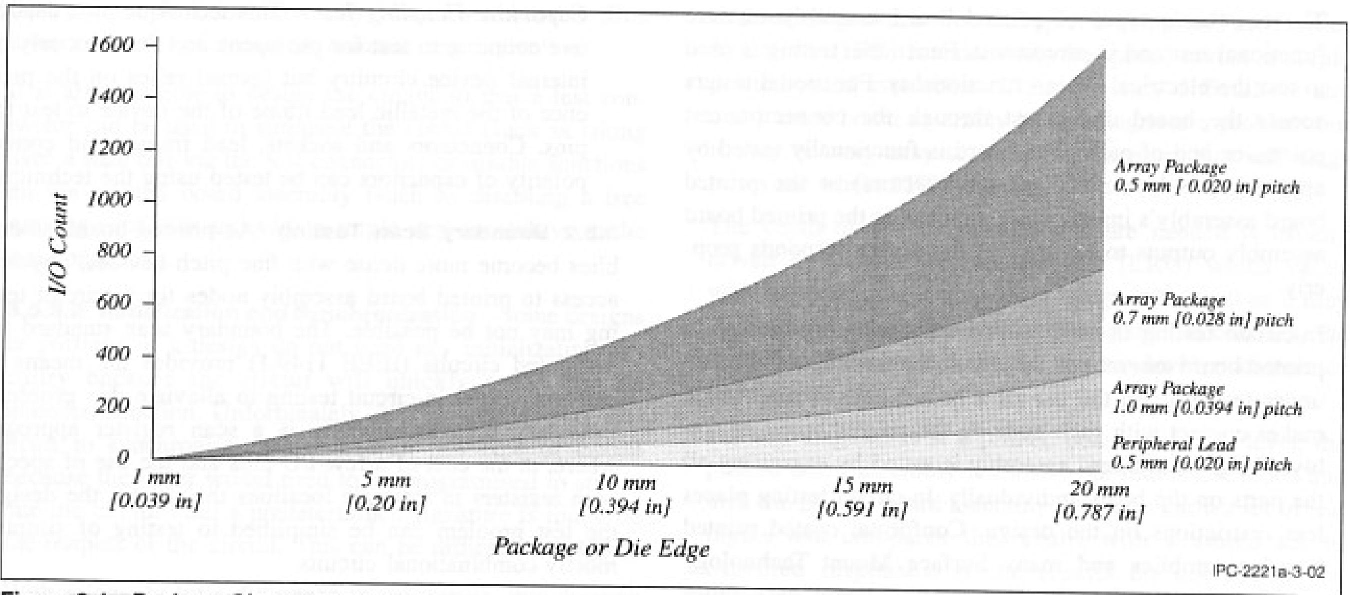


Figure 3-1 Package Size and I/O Count

All mechanical parts appearing on the assembly pictorial **shall** be assigned an item number which **shall** match the item number assigned on the parts list.

Electrical components, such as capacitors, resistors, fuses, ICs, transistors, etc., **shall** be assigned reference designators, (Ex. C5, CR2, F1, R15, U2, etc.). Assignment of electrical reference designators **shall** be the same as (match) those assignments given to the same components on the Logic/schematic diagram.

It is advisable to group like items; e.g., resistors, capacitors, ICs, etc., in some sort of ascending or numerical order.

The parts list may be handwritten, manually typed on to a standard format, or computer generated.

3.5 Test Requirement Considerations Normally, prior to starting a design, a testability review meeting should be held with fabrication, assembly, and testing. Testability concerns, such as circuit visibility, density, operation, circuit controllability, partitioning, and special test requirements and specifications are discussed as a part of the test strategy. See Appendix A for a checklist of design for testability criteria.

During the design testability review meeting, tooling concepts are established, and determinations are made as to the most effective tool-cost versus board layout concept conditions.

During the layout process, any circuit board changes that impact the test program, or the test tooling, should immediately be reported to the proper individuals for determination as to the best compromise. The testing concept should develop approaches that can check the board for problems, and also detect fault locations wherever possible. The test concept and requirements should economically facilitate the detection, isolation, and correction of faults of the design verification, manufacturing, and field support of the printed board assembly life cycle.

3.5.1 Printed Board Assembly Testability Design of a printed board assembly for testability normally involves systems level testability issues. In most applications, there are system level fault isolation and recovery requirements such as mean time to repair, percent up time, operate through single faults, and maximum time to repair. To meet the contractual requirements, the system design may include testability features, and many times these same features can be used to increase testability at the printed board assembly level. The printed board assembly testability philosophy also needs to be compatible with the overall integrations, testing and maintenance plans for the contract. The factory testers to be used, how integration and test is planned, when printed board assemblies are conformal coated, the depot and field test equipment capabilities and personnel skill level are all factors that must be considered when developing the printed board assembly test strategy. The test philosophy may be different for different phases of the program. For example, the first unit debug philosophy may be much different than the test philosophy for spares when all the systems have already been shipped.

Before the PCB design starts, requirements for the system testability functions should be presented at the conceptual design review. These requirements and any derived requirements should be partitioned down to the various printed board assemblies and documented. The system and program level test criteria and how they are partitioned down to the printed board assembly requirements are beyond the scope of this document. Appendix A provides an example of a checklist to be used in evaluating the testability of the design.

The two basic types of printed board assembly test are functional test and in-circuit test. Functional testing is used to test the electrical design functionality. Functional testers access the board under test through the connector, test points, or bed-of-nails. The board is functionally tested by applying pre-determined stimuli (vectors) at the printed board assembly's inputs while monitoring the printed board assembly outputs to ensure that the design responds properly.

In-circuit testing is used to find manufacturing defects in printed board assemblies. In-circuit testers access the board under test through the use of a bed-of-nails fixture which makes contact with each node on the printed board assembly. The printed board assembly is tested by exercising all the parts on the board individually. In-circuit testing places less restrictions on the design. Conformal coated printed board assemblies and many Surface Mount Technology (SMT) and mixed technology printed board assemblies present bed-of-nails physical access problems which may prohibit the use of in-circuit testing. Primary concerns for in-circuit test are that the lands or pins (1) must be on grid (for compatibility with the use of bed-of-nails fixture) and (2) should be accessible from the bottom side (a.k.a. non-component or solder side of through-hole technology boards) of the printed board assembly.

Manufacturing Defects Analyzer (MDA) provide a low cost alternative to the traditional in-circuit tester. Like the in-circuit tester, the MDA examines the construction of the printed board assembly for defects. It performs a subset of the types of tests, mainly only tests for shorts and opens faults without power applied to the printed board assembly. For high volume production with highly controlled manufacturing processes (i.e., Statistical Process Control techniques), the MDA may have application as a viable part of a printed board assembly test strategy.

Vectorless Test is another low cost alternative to in-circuit testing. Vectorless Test performs testing for finding manufacturing process-related pin faults for SMT boards and does not require programming of test vectors. It is a powered-off measurement technique consisting of three basic types of tests:

1. *Analog Junction Test* – DC current measurement test on unique pin pairs of the printed board assembly using the ESD protection diodes present on most digital and mixed signal device pins.
2. *RF Induction Test* – Magnetic induction is used to test for device faults utilizing the printed board assemblies devices protection diodes. This technique uses chips power and ground pins to make measurements for finding solder opens on device signal paths, broken bond wires, and devices damaged by ESD. Parts incorrectly oriented can also be detected. Fixturing containing magnetic inducers are required for this type of test.
3. *Capacitive Coupling Test* – This technique uses capacitive coupling to test for pin opens and does not rely on internal device circuitry but instead relies on the presence of the metallic lead frame of the device to test the pins. Connectors and sockets, lead frames and correct polarity of capacitors can be tested using the technique.

3.5.2 Boundary Scan Testing As printed board assemblies become more dense with fine pitch devices, physical access to printed board assembly nodes for in-circuit testing may not be possible. The boundary scan standard for integrated circuits (IEEE 1149.1) provides the means to perform virtual in-circuit testing to alleviate this problem. Boundary scan architecture is a scan register approach where, at the cost of a few I/O pins and the use of special scan registers in strategic locations throughout the design, the test problem can be simplified to testing of simpler, mostly combinational circuits.

In many applications, the inclusion of scan registers on the inputs and outputs of the printed board assembly allows the board to be tested while installed. If the circuit is more complex, additional sets of scan registers can be included in the design to capture intermediate results and apply test vectors to exercise portions of the design.

A full description of the standard access port and boundary scan architecture can be found in IEEE 1149.1. The full test access port capabilities are not needed to gain significant testability via the scan registers.

The decision to use boundary scan test as part of a test strategy should consider the availability of boundary scan parts and the return on investment for capital equipment and software tools required for implementing this test technique. Boundary scan testing can be conducted using a low cost PC-based tester which requires access to the printed board assembly under test through the edge connector or an existing functional, in-circuit, or hybrid tester that may be adapted to perform boundary scan testing.

3.5.3 Functional Test Concern for Printed Board Assemblies There are several concerns for designing the printed board assembly for functional testability. The use of test connectors, problems with initialization and synchronization, long counter chains, self diagnostics, and physical testing are topics which are discussed in detail in the following subsections and are not meant to be tutorials on testability but rather ideas of how to overcome typical functional testing problems.

3.5.3.1 Test Connectors Fault isolation on conformal coated boards or most SMT and mixed technology designs can be very difficult because of the lack of access to the circuitry on the board.

If strategic signals are brought out to a test connector or an area on the printed board where the signals can be probed

(test points), fault isolation may be much improved. This lowers the cost of detection, isolation and correction.

It is also possible to design the circuit so that a test connector can be used to stimulate the circuit (such as taking over a data bus via the test connector) or disable functions on the printed board assembly (such as disabling a free running oscillator and adding single step capability via the test connector).

3.5.3.2 Initialization and Synchronization Some designs or portions of a design do not need any initialization circuitry because the circuit will quickly cycle into its intended function. Unfortunately, it is sometimes very difficult to synchronize the tester with this type of circuit because the tester would need to be programmed to stimulate the circuit until a predetermined signature is found on the outputs of the circuit. This can be difficult to achieve.

With relatively little difference in the design, initialization capability can usually be designed into the circuitry allowing the printed board assembly to be quickly initialized and the circuit and the tester can follow the expected outputs of the printed board assembly.

Free running oscillators also present a problem in testing because of the synchronization problem with the test equipment. These problems can be overcome by (1) adding test circuitry to select a test clock instead of the oscillator; (2) removing the oscillator for test and injecting a test clock; (3) overriding the signal; or (4) designing the clock system so that the clocking can be controlled via a test connector or test points.

3.5.3.3 Long Counter Chains Long counter chains in the design with signals used from many stages of the counter chain present another testability problem. Testability can be very bad if there is no means to preset the counter chain to different values to facilitate testing of the logic that is driven from the high order stages of the counter chain.

Testability is much improved if the counter chain is either broken into smaller counter chains (perhaps no more than 10 stages) which can be individually controlled or if the counter chain can be loaded via the test software. The test software can then verify the operation of the logic that is driven from the counter stages without wasting the simulation and test time that would be required to clock through the complete counter chain.

3.5.3.4 Self Diagnostics Self diagnostics are sometimes imposed either contractually or via derived requirements. Careful consideration should be given to determine how to implement these requirements.

Many times a printed board assembly does not contain functions that lend themselves to self diagnostics at the printed board assembly level but a small group of printed board assemblies, when taken as a unit, do lend themselves to good diagnostics. For example, a complex Fast Fourier Transform (FFT) function may be spread across multiple printed board assemblies. It may be very difficult for any one printed board assembly to self diagnose a problem but it may be very easy to design-in circuitry that self diagnoses the whole FFT function.

The depth of self diagnostics that are needed is usually driven by the line replaceable unit (LRU) which varies with requirements. It may be an integrated circuit or it may be a drawer of electronics depending on the contract, the function of the design, or the system level maintenance philosophy.

For self diagnostics at a printed board assembly level, the printed board assembly is usually put into a test mode and then the printed board assembly applies a known set of test inputs and compares the results with a stored set of expected responses. If the results do not match the expected responses, the printed board assembly signals the test equipment indicating the printed board assembly failed the self-test. There are many variations on this scheme. Some examples are:

1. The printed board assembly is placed in a feedback loop with the results checked after a predetermined number of cycles.
2. A special test circuit or the Central Processor Unit (CPU) applying the stimuli and comparing the signature of the responses against a known pattern.
3. The printed board assembly performing self-checks when idling and then supplying the results to another (or diagnostic) printed board assembly for verification of the responses, etc.

3.5.3.5 Physical Test Concerns Printed board assembly functional test equipment is usually very expensive and requires highly skilled personnel to operate. If printed board assembly testability is poor, the printed board assembly test operation can be very expensive. There are some simple physical considerations that can decrease the debug time and therefore the overall test costs.

The orientation of polarized parts should be consistent so that the operator does not get confused with parts being oriented 180° out of phase with other parts on the printed board assembly. Nonpolarized parts still need to have the pin #1 identified so that the test operator knows which end to probe when guided probe software says to probe a specific pin.

Test connectors are much preferred over test points which require the use of test clips or test hook-up wires. However, test points such as riser leads are preferred over clipping on to the lead of a part. If riser leads are used for temporary testing, such as determining a select-by-test resistor, it is suggested that the risers remain after the installation of the selected component. This allows verification of the selected item without re-fixturing the assembly.

Signals that are not accessible for probing (such as can happen with leadless parts) can greatly increase fault isolation problems. If scan registers are not used, it is recommended that every signal have a land or other test point somewhere on the printed board assembly where the signal can be probed. It is also recommended that lands used for test points be located on grid and placed so that all the probing can be done from the secondary side of the printed board assembly. If it is not feasible to provide capability for probing every signal, then (1) only the strategic signals should have special probing locations and (2) the test vectors need to be increased or other test techniques need to be utilized to assign fault isolation to one component or a small set of components.

Many faults are often due to shorts between the leads of adjacent parts, shorts between a part lead and an external layer conductor on the printed board or shorts between two printed board conductors on the external layers of the printed board. The physical design must consider these normal manufacturing defects and not impair the isolation of the faults due to lack of access or inconvenient access to signals. As with design for in-circuit testability, probe pad test points should be on grid to allow automated probing to be used in the future.

Partitioning of the design into functions, perhaps digital separated from analog, is sometimes required for electrical performance. Testing concerns also are helped with physical separation of dissimilar functions. Separation of not just the circuitry but also the test connectors or at least grouping the pins on the connectors can help improve testability. Designs that mix digital design with high performance analog design may require testing on two or more sets of test equipment. Separating the signals will not only help the test fixturing but will help the operator in debugging the printed board assembly.

As with in-circuit test fixturing, functional test fixturing can have a significant cost impact. Normally a standard board size or only a few board sizes are used for all designs on a program. Similarly one, or at most a few, test fixtures are typically used for a program. Generating test fixtures can be costly and debugging noise problems in the fixtures or tuning the fixtures to the tester can be expensive. If the test fixturing is not adequately engineered, it may not be possible to accurately measure the board under test. Typically much effort is expended in generating a few test fixtures and it is expected that the fixtures will be used for all the printed board assembly designs. Therefore the test fixturing restrictions must be considered in the printed board assembly design. The fixturing restraints can be significant. Such as (1) requiring ground and voltage supplies on specific connector pins, (2) limiting which pins can be used for high speed signals, (3) limiting which pins can be used for low noise applications, (4) defining power switching limitations, (5) defining voltage and current limitations on each pin, etc.

3.5.4 In-Circuit Test Concerns for Printed Board Assemblies In-circuit testing is used to find shorts, opens, wrong parts, reversed parts, bad devices, incorrect assembly of printed board assemblies and other manufacturing defects. In-circuit testing is neither meant to find marginal parts nor to verify critical timing parameters or other electrical design functions.

In-circuit testing of digital printed board assemblies can involve a process that is known as backdriving (see IPC-T-50). Backdriving can also cause devices to oscillate and the tester can have insufficient drive to bring a device out of saturation. Backdriving can be performed only for controlled periods of time, or the junction of the device (with the overdriven output) will overheat.

The two main concerns for designing the printed board and printed board assembly for in-circuit testability are design for compatibility with in-circuit test fixturing and electrical design considerations. These topics are discussed in detail in the following subsections.

3.5.4.1 In-Circuit Test Fixtures In-circuit test fixtures are commonly called bed-of-nails fixtures. A bed-of-nails fixture is a device with spring contact probes which contact each node on the board under test. The following guidelines should be followed during printed board assembly layout to promote in-circuit testability in bed-of-nails fixtures:

1. The diameter of lands of plated-through holes and vias used as test lands are a function of the hole size (see 9.1.1). The diameter of test lands used specifically for probing should be no smaller than 0.9 mm [0.0354 in]. It is feasible to use 0.6 mm [0.0236 in] diameter test lands on boards under 7700 mm^2 [11.935 in^2].
2. Clearances around test probe sites are dependent on assembly processes. Probe sites should maintain a clearance equal to 80% of an adjacent component height with a minimum of 0.6 mm [0.0236 in] and a maximum of 5 mm [0.20 in] (see Figure 3-2).
3. Part height on the probe side of the board must not exceed 5.7 mm [0.224 in]. Taller parts on this side of the board will require cutouts in the test fixture. Test lands should be located 5 mm [0.20 in] away from tall components. This allows for test fixture profiling tolerances during test fixture fabrication (see Figure 3-3).
4. No parts or test lands are to be located within 3 mm of the board edges.
5. All probe areas must be solder coated or covered with a conductive nonoxidizing coating. The test lands must be free of solder resist and markings.

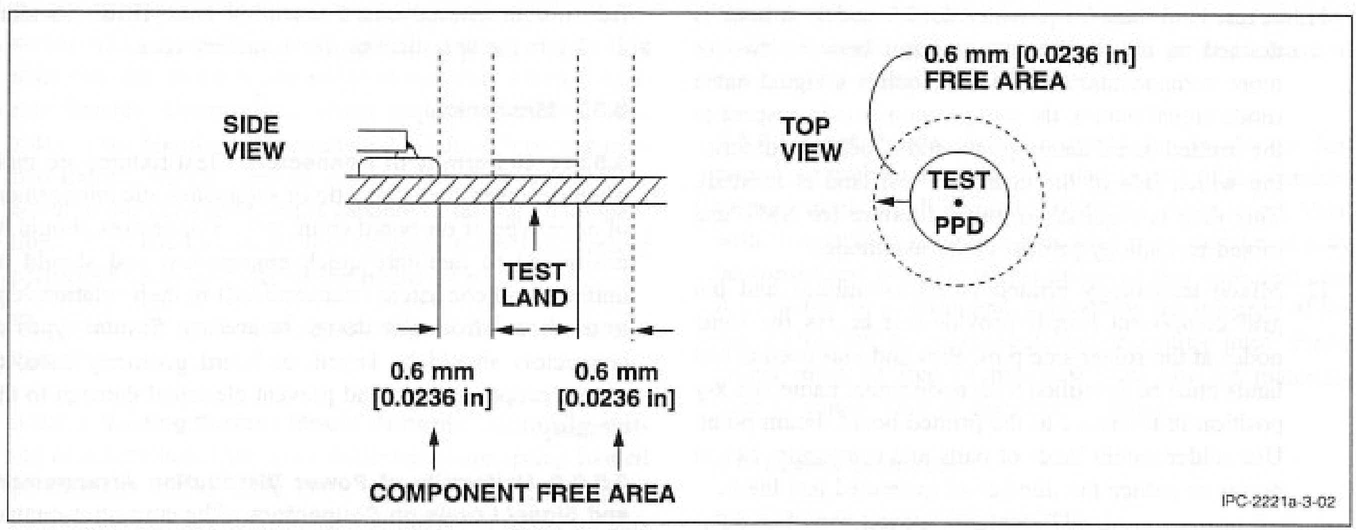


Figure 3-2 Test Land Free Area for Parts and Other Intrusions

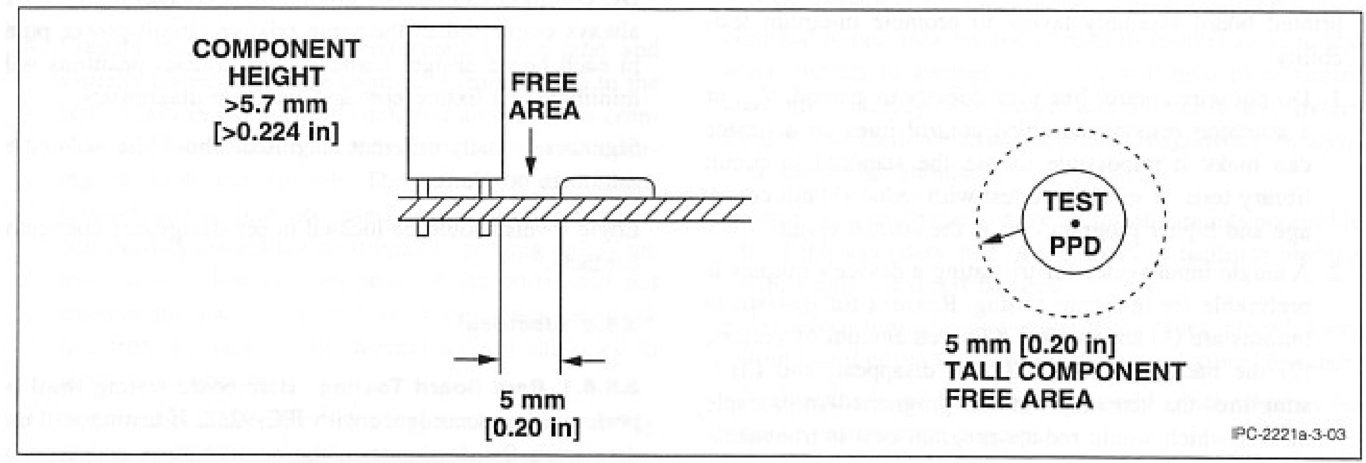


Figure 3-3 Test Land Free Area for Tall Parts

6. Probe the test lands or vias, not the termination/castellations of leadless surface mount parts or the leads of leaded parts (see Figure 3-4). Contact pressure can cause an open circuit or make a cold solder joint appear good.
7. Avoid requiring probing of both sides of the printed board. Use vias, to bring test points to one side, the bottom side (noncomponent or solder side of through-hole technology printed board assemblies) of the board. This allows for a reliable and less expensive fixture.
8. Test lands should be on 2.5 mm [0.0984 in] hole centers, if possible, to allow the use of standard probes and a more reliable fixture.
9. Do not rely on edge connector fingers for test lands. Gold plated fingers are easily damaged by test probes.
10. Distribute the test lands evenly over the board area. When the test lands are not evenly distributed or when they are concentrated in one area, the results are board flexing, probing faults, and vacuum sealing problems.

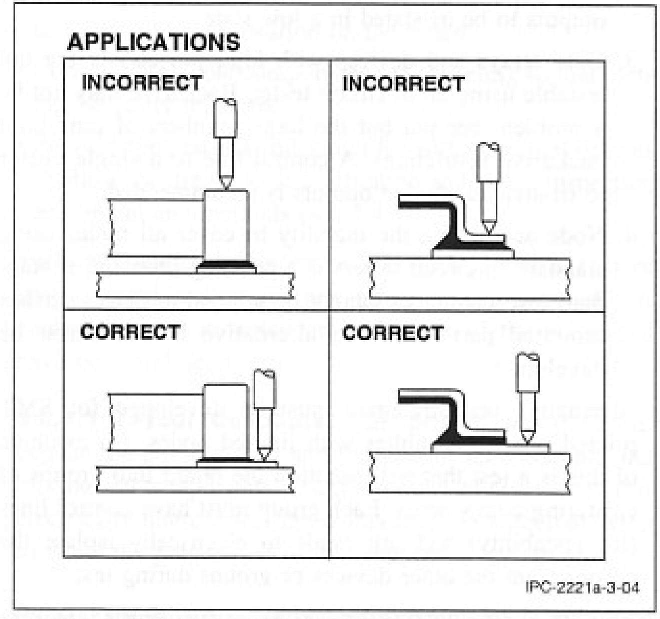


Figure 3-4 Probing Test Lands

11. A test land must be provided for all nodes. A node is defined as an electrical connection between two or more components. A test land requires a signal name (node signal name), the x-y position axis in respect to the printed board datum point, and a location (describing which side of the board the test land is located). This data is required to build a fixture for SMT and mixed technology printed board assemblies.
12. Mixed technology printed board assemblies and pin grid component boards provide test access for some nodes at the solder side pins. Pins and vias used at test lands must be identified with node signal name and x-y position in reference to the printed board datum point. Use solder mount lands of parts and connectors as test points to reduce the number of generated test lands.

3.5.4.2 In-Circuit Electrical Considerations The following electrical considerations should be followed during printed board assembly layout to promote in-circuit testability:

1. Do not wire control line pins directly to ground, V_{cc}, or a common resistor. Disabled control lines on a device can make it impossible to use the standard in-circuit library tests. A specialized test with reduced fault coverage and higher program cost is the normal result.
2. A single input vector for tri-stating a device's outputs is preferable for in-circuit testing. Reasons for tri-statable outputs are (1) testers have a limited amount of vectors, (2) the backdrive problems will disappear, and (3) it simplifies the generation of test programs. An example of this which would reduce program cost is tri-statable Programmable Array Logic (PAL) outputs. Use a spare input to a pull-up resistor plus an equation that would enable a normal function in a high state and the device outputs to be tri-stated in a low state.
3. Gate arrays and devices with high pin counts are not testable using an in-circuit tester. Backdrive may not be a problem per pin but the large numbers of pins limit backdrive restrictions. A control line or a single vector to tri-state all device outputs is recommended.
4. Node access and the inability to cover all nodes using standard in-circuit testers is a growing problem. If standard test techniques cannot be applied to detect surface mounted part faults, an alternative method must be developed.

Alternative test strategies must be developed for SMT printed board assemblies with limited nodes. An example of this is a test that will partition the board into groups of clustering components. Each group must have control lines (for testability) and test lands to electrically isolate the cluster from the other devices or groups during test.

Another alternative test method for opens, shorts, and correct devices is boundary scan. This built-in-test-circuitry (electronic bed-of-nails) is gaining momentum in the surface mount printed board assembly area. IEEE Standard 1149.1 is the specification for boundary scan.

3.5.5 Mechanical

3.5.5.1 Uniformity of Connectors Test fixtures are most often designed for automatic or semiautomatic engagement of edge type or on-board connectors. Connectors should be positioned to facilitate quick engagement and should be uniform and consistent (standardized) in their relationships to the board from one design to another. Similar types of connectors should be keyed, or board geometry used, to ensure proper mating, and prevent electrical damage to the circuitry.

3.5.5.2 Uniformity of Power Distribution Arrangement and Signal Levels on Connectors The connector contact position should be uniform for AC and DC power levels, DC common and chassis ground, e.g., contact number 1 is always connected to the same relative circuit power point in each board design. Standardizing contact positions will minimize test fixture cost and facilitate diagnostics.

Signals of widely different magnitude should be isolated to minimize crosstalk.

Logic levels should be located in pre-designated connector contacts.

3.5.6 Electrical

3.5.6.1 Bare Board Testing Bare board testing **shall** be performed in accordance with IPC-9252. If testing will use data from the design area, the configuration and type of data provided will be determined by the method of test selected.

Bare board testing is performed by the printed board supplier and includes continuity, insulation resistance and dielectric withstanding voltage. Suppliers can also perform testing of controlled impedance circuitry. Continuity tests are performed to assure conductors are not broken (opens) or inadvertently connected together (shorts). Insulation resistance and dielectric withstanding voltage testing is performed to assure sufficient conductor spacing and dielectric thickness.

There are two basic types of continuity testing; Golden Board and Intelligent. In Golden Board test, a known good board is tested and its results are used to test all the remaining boards in the lot. If there were an error in the Golden Board, an error in all boards could go undetected. The Intelligent test verifies each board against the design's electrical net list. It will not miss the defects which could be undetected in a Golden Board test.

Designs which do not have all electrical connections available from one side of the board (such as boards with blind or buried vias, components on both sides with via holes

solder resist tented or boards bonded to both sides of heat-sinks) will require Flip or Clamshell testing. Flip testing tests one side of the board and then the other on two separate fixtures. Connections which require contacting both sides of the board are not evaluated. Clamshell testing uses two fixtures which come in contact with both sides of the board at the same time and is capable of testing all connections. Flip and Clamshell testing costs more than testing performed from one side of the board only.

The following areas **shall** be considered before starting a design.

3.5.6.2 Testing Surface Mount Patterns Normally, testing of a bare board involves fixturing where spring loaded pins contact plated holes. On a surface mount pattern, the ends of the nets are typically not at holes but rather on surface mount lands. There are at least two different strategies for performing testing:

A. Contact the via which is connected to the land and visually inspect to ensure continuity from the via to the land. Vias can be designed such that they are on a common grid which will reduce the need for special fixturing for each part number. The barrels of the plated-through holes that are used for internal electrical connectivity should not be subject to probing unless the force is very low and the point of the probe will not damage the barrel. These barrels can crack or break free from the land on the internal layer if subjected to mechanical stresses.

B. Test to the land itself. This approach will probably require special fixturing since surface mount lands may not all be on a grid. Additionally, computer design systems may place the end-of-net point at a via rather than the land which may require adjustment of test point locations.

3.5.6.3 Testing of Paired Printed Boards Laminated to a Core At least two approaches are available for electrical test:

A. Test the top and bottom of the laminated composite printed board separately. If there are plated holes which provide a side-to-side interconnection, they will require a manual electrical test or visual inspection to ensure hole continuity.

B. Use a clam shell type fixture where both the top and bottom of the composite printed board can be tested together. The use of the first approach will require that the electrical test data be provided in two parts. When networks have terminations on both sides of the printed board, the electrical test data should be split into at least two parts with the end of net occurring at the side-to-side interconnect. "Self learn" testing from a known good board will provide the data automatically in the above format.

3.5.6.4 Point of Origin Electrical test and numerical control data should have a common origin point for ease of constructing electrical test fixtures.

3.5.6.5 Test Points When required by the design, test points for probing **shall** be provided as part of the conductor pattern and **shall** be identified on the drawing set. Vias, wide conductors, or component lead mounting lands may be considered as probe points provided that sufficient area is available for probing and maintaining the integrity of the via, conductor, or component lead mounting joint. Probe points must be free of nonconductive coating materials such as solder resist or conformal coating.

3.6 Layout Evaluation

3.6.1 Board Layout Design The design layout from one board design to another should be such that designatedareas are identified by function, e.g., power supply section confined to one area, analog circuits to another section, and logic circuits to another, etc. This will help to minimize crosstalk, simplify bare board and assembly test fixture design, and facilitate troubleshooting diagnostics. In addition, the design should:

- Ensure that components have all testable points accessible from the secondary side of the board to facilitate probing with single-sided test fixtures.
- Have feed-throughs and component holes placed away from board edges to allow adequate test fixture clearance.
- Require the board be laid out on a grid which matches the design team testing concept.
- Allow provision for isolating parts of the circuit to facilitate testing and diagnostics.
- Where practical, group test points and jumper points in the same physical location on the board.
- Consider high-cost components for socketing so that parts can be easily replaced.
- Provide optic targets (fiducials) for surface mount designs to allow the use of optic positioning and visual inspection equipment and methods (see 5.4.3).

Surface mounted components and their patterns require special consideration for test probe access, especially if components are mounted on both sides of the board and have very high lead counts.

3.6.1.1 Layout Concepts The printed board layout depicts the physical size and location of all electronic and mechanical components, and the routing of conductors that electrically interconnect the components in sufficient detail to allow the preparation of documentation and artwork.

3.6.2 Feasibility Density Evaluation After approved documents for schematic/logic diagrams, parts lists, and end-product and testing requirements are provided, and

before the actual drawing of the layout is begun, a feasibility density evaluation should be made. This should be based on the maximum size of all parts required by the parts list and the total space they and their lands will require on the board, exclusive of interconnection conductor routing.

The total board geometry required for this mounting and termination of the components should then be compared to the total usable board area for this purpose. Reasonable maximum values for this ratio are 70% for Level A, 80% for Level B, and 90% for Level C. Component density values higher than these will be a cause for concern. The lower these values are, the easier it will be to design a cost-effective functional board.

Figure 3-5 provides the usable board area for the standardized board sizes recommended in Figure 5-1.

Table 3-2 gives the area (in 0.5 mm [0.020 in] grid elements) a component will occupy on the board for a variety of components. As an example, the 14 lead dual in-line package for through-hole technology occupies a total of 84.0 grid elements. The package outline that encloses the component and land pattern has a grid matrix of 20 x 42 grid elements on 0.5 mm [0.020] centers. The 20 grid elements establish an outline dimension of 10 mm [0.394 in] while the 42 grid elements account for 21 mm [0.827 in]. This component area would use up a portion of the board usable area. The component outline does not include grid elements for conductor routing outside the land area. Total component area compared to total usable area provides the conductor routing availability and thus the density percentage.

An alternative method of feasibility density evaluation expresses board density in units of square centimeters per

Board Size (Fig. 5-1)	Overall Dimensions Height mm [in]	Overall Dimensions Width mm [in]	Usable Dimensions Height mm [in]	Usable Dimensions Width mm [in]	Usable Area mm^2	Usable Area Grid Elements 0.5 mm Grid	Usable Area cm^2
A1	80 [3.15]	60 [2.36]	65 [2.56]	50 [1.97]	3200	12800	32
B1	170 [6.692]		155 [6.102]		7700	30800	77
C1	260 [10.25]		245 [9.646]		12200	48800	122
D1	350 [13.78]		335 [13.19]		16700	66800	167
A2	80 [3.15]	120 [4.724]	65 [2.56]	110 [4.331]	7100	28400	71
B2	170 [6.692]		155 [6.102]		17000	68000	170
C2	260 [10.25]		245 [9.646]		26900	107600	269
D2	350 [13.78]		335 [13.19]		36800	147200	368
A3	80 [3.15]	180 [7.087]	65 [2.56]	170 [6.693]	11000	44000	110
B3	170 [6.692]		155 [6.102]		26300	105200	263
C3	260 [10.25]		245 [9.646]		41600	166400	416
D3	350 [13.78]		335 [13.19]		56900	227600	569
A4	80 [3.15]	240 [9.449]	65 [2.56]	230 [9.055]	14900	59600	149
B4	170 [6.692]		155 [6.102]		35600	142400	356
C4	260 [10.25]		245 [9.646]		56300	225200	563
D4	350 [13.78]		335 [13.19]		77000	308000	770

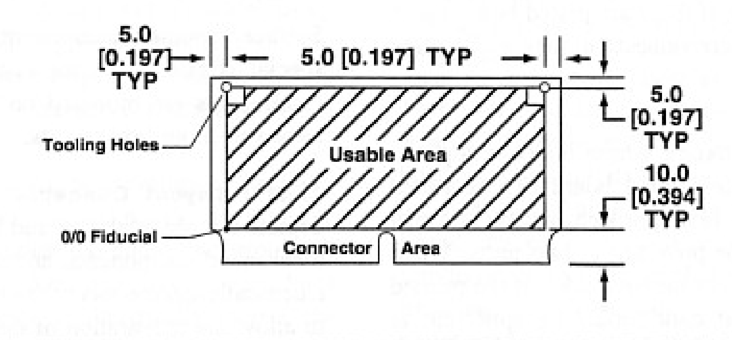


Figure 3-5 Example of Usable Area Calculation, mm [in] (Usable area determination includes clearance allowance for edge-board connector area, board guides, and board extractor.)

Table 3-2 Component Grid Areas

Component Description	Type[1]	Number of Grid Elements[2] 0.5 mm [0.20 in] Grid	
D07 (without stress relief loop)	THT	6 x 24	144
D07 (with stress relief loop)	THT	6 x 28	168
T05	THT	20 x 20	400
T024	THT	10 x 10	100
CK05	THT	6 x 12	72
CM05, 13000pF	THT	20 x 44	880
CM06, 400pF	THT	12 x 26	312
RC07	THT	6 x 20	120
RC20	THT	10 x 26	260
RN60	THT	10 x 30	300
CQFP-10 T090	SMT	16 x 12	192
CQFP-28	SMT	34 x 34	1156
CQFP-144	SMT	68 x 68	4624
3216 (1206)	SMT	4 x 10	40
4564 (1825)	SMT	14 x 12	168
6032	SMT	8 x 18	144
DIP-14	THT	20 x 42	840
DIP-14	SMT	22 x 42	924
DIP-24	SMT	22 x 60	1320
DIP-24L	SMT	26 x 64	1664
SOD87/MLL-41	SMT	6 x 14	84
SOT23	SMT	8 x 8	64
SOT89	SMT	12 x 10	120
SOT143	SMT	8 x 8	64
SQFP 7x7-40	SMT	22 x 22	484
SOIC-20W	SMT	28 x 24	672
SOIC-36X	SMT	48 x 24	1152
TSOP 10x20	SMT	22 x 44	968
SOJ 26/350	SMT	24 x 34	816

[1]THT = Through-Hole Technology, SMT = Surface Mount Technology
[2]Grid area includes physical component outlines and land areas. It does not include space for conductor routing.

equivalent SOIC. A 16-pin SOIC occupies approximately one cm^2 of board area. Figure 3-6 shows a table for determining the SOIC equivalent for a variety of components and the total SOIC equivalents used on the board. This number is then divided into the total square centimeters of usable board area. Reasonable maximum density values are 0.55 cm^2 per SOIC for Level A, 0.50 for Level B, and 0.45 for Level C. Density values can increase with additional circuit layers. Also, when using surface mount technology, the potential usable board area is theoretically doubled.

3.7 Performance Requirements Finished printed boards **shall** meet the performance requirements of IPC-6011 and its applicable sectional specification.

Sheet 1 of 1

PRINTED BOARD DENSITY EVALUATION			Date of issue	No. / Revised
DESCRIPTION: SOICs per square centimeter				
Comp. name	# of comp.	or	IC equiv	Comments
8 SOIC		.50		
14 SOIC		1.00		
16 SOIC		1.00		
16L SOIC		1.00		
20 SOIC		1.25		
24 SOIC		1.50		
28 SOIC		1.75		
18 PLCC		1.13		
18L PLCC		1.13		
20 PLCC		1.25		
28 PLCC		1.75		
44 PLCC		2.75		
52 PLCC		3.25		
68 PLCC		4.25		
84 PLCC		5.25		
SOT 23		0.19		
SOT 89		0.19		
SOMC 1401		1.00		
SOMC 1601		1.00		
2012 (0805)		0.13		
3216 (1206)		0.13		
3225 (1210)		0.13		
4564 (1812)		0.13		
MLL 34		0.13		
MLL 41		0.13		
others (specify)				

Total IC equivalent ________________

Total board area	(X)	=	cm² cm²
Usable board area	(X)	=	Usable board area Design criteria

☐ Analog	☐ Digital
Etch & Spac.	/
PWB & GYD Sz	/

Devel. by	Date	App'd by	Date

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Figure 3-6 Printed Board Density Evaluation

4 MATERIALS

4.1 Material Selection A designer of printed boards has several material choices to consider, ranging from standard to highly sophisticated and specialized. When specifying materials, the designer must first determine what requirements the printed board must meet. These requirements include temperature (soldering and operating), electrical properties, interconnections (soldered components, connectors), structural strength, and circuit density. It should be noted that increased levels of sophistication may lead to increased material and processing costs.

When constructing a composite from materials with different temperature characteristics, the maximum end-use temperature allowable must be limited to that of the lowest rated material.

Other items that may be important in the comparison of various materials include:

Resin Formula,
Flame Resistance,
Thermal Stability,
Structural Strength,
Electrical Properties,
Flexural Strength,
Maximum Continuous Safe Operating Temperature,
Glass Transition Temperature (T_g),
Reinforcing Sheet Material,
Nonstandard Sizes and Tolerances,
Machinability or Punchability,
Coefficients of Thermal Expansion (CTE),
Dimensional Stability, and
Overall Thickness Tolerances.

4.1.1 Material Selection for Structural Strength The first design step in the selection of a laminate is to thoroughly define the service requirements that must be met, i.e., environment, vibration, "G" loadings, shock (impact), physical and electrical requirements.

The choice of laminate should be made from standard materials to avoid costly and time consuming proof-out tasks. Several laminates may be candidates, and the choice should be optimized to obtain the best balance of properties.

Materials should be easily available in the form and size required. Special laminate may be costly, and have long lead times. Special laminates should be analyzed against all of the parameters discussed in this section.

Items to be considered are such things as machining, processing, processing costs, and the overall specification of the raw material.

In addition to these parameters, the structural strength of the board must be able to withstand the assembly and operational stresses.

4.1.2 Material Selection for Electrical Properties Some of the critical properties to consider are electrical strength, dielectric constant, moisture resistance, and hydrolytic stability. Table 4-1 lists properties of some of the more common systems. Consult the laminate manufacturer utilized by the fabricator for specific values.

4.1.3 Material Selection for Environmental Properties Table 4-2 shows the properties affected by the environment for some of the more common resin systems. The stated values are typical and will vary among different material suppliers. Consult the laminate manufacturer utilized by the fabricator for specific values.

4.2 Dielectric Base Materials (Including Prepregs and Adhesives) Bonding materials described in the following paragraphs **shall** be used to bond layers of copper foil, bare laminate, copper clad laminate or heat-sinking planes to each other.

4.2.1 Preimpregnated Bonding Layer (Prepreg) Prepreg **shall** conform to the types listed in IPC-4101 or UL 746E. In most cases, the prepreg should be of the same resin and reinforcement type as the copper clad laminate. The reinforcement style, nominal resin flow, nominal scaled flow thickness, nominal gel time, and nominal resin content are process parameters normally dictated by the printed board manufacturing process.

Unless design constraints dictate, these values **shall** not be included on master drawings, but **shall** only be specified and used in procurement specifications by the printed board manufacturer.

4.2.2 Adhesives Adhesives used in printed board assemblies are drawn from at least five basic resin types covering a wide range of properties. In addition to adhesion quality or bond strength, criteria for adhesive selection include hardness, coefficient of thermal expansion (CTE), service temperature range, dielectric strength, cure conditions and tendency for outgassing. In some cases structural adhesives may be sufficient for thermal bonding applications, see 4.2.5. Each adhesive type has both strong and weak points.

Selection of a resin system for an adhesive or encapsulant is to be based on the characteristics of the materials being bonded and their compatibility. Special treatments, such as primers or activators, may be required to suitably activate surfaces for bonding. The selection process should also consider the exact purpose of the adhesive bond and its use environment. Fungus inert materials are also a consideration. Not all adhesives are suitable for direct application on or near electronic products due to either their chemical or dielectric properties. Incorrect selection of materials may result in product degradation or failure.

Table 4-1 Typical Properties of Common Dielectric Materials

Property	Material					
	FR-4 (Epoxy E-glass)	Multi-functional Epoxy	High Performance Epoxy	Bismalaimide Triazine/ Epoxy	Polyimide	Cyanate Ester
Dielectric Constant (neat resin)	3.9	3.5	3.4	2.9	3.5 - 3.7	2.8
Dielectric Constant (reinforcement/resin)[1]	—	—	—	—	—	—
Electric Strength[2] (V/mm)	39.4 x 10^3	51.2 x 10^3	70.9 x 10^3	47.2 x 10^3	70.9 x 10^3	65 x 10^3
Volume Resistivity (D-cm)	4.0 x 10^6	3.8 x 10^6	4.9 x 10^6	4 x 10^6	2.1 x 10^6	1.0 x 10^6
Water Absorption (wt%)	1.3	0.1	0.3	1.3	0.5	0.8
Dissipation Factor (DX)	0.022	0.019	0.012	0.015	0.01	0.004

[1]For values of dielectric constant, see Table 6-2.
[2]The stated electrical strength values are commonly evaluated under test conditions with a 0.125 mm [0.004921 in] core laminate thickness. These values should not be considered linear for high voltage designs with a minimum dielectric separation, i.e., less than 0.09 mm [0.00354 in].

Table 4-2 Environmental Properties of Common Dielectric Materials

Environmental Property	Material					
	FR-4 (Epoxy E-glass)	Multi-functional Epoxy (E-glass)	High Performance Epoxy (E-glass)	Bismalaimide Triazine/ Epoxy	Polyimide (E-glass)	Cyanate Ester
Thermal Expansion xy-plane (ppm/°C)	16 - 19	14 - 18	14 - 18	~15	8 - 18	~15
Thermal Expansion z-axis below T_g[3] (ppm/°C)	50 - 85	44 - 80	~44	~70	35 - 70	81
Glass Transition Temp. T_g (°C)	110 - 140	130 -160	165 - 190	175 - 200	220 - 280	180 - 260
Flexural Modulus (x 10^{10} Pa) Fill[1]	1.86	1.86	1.93	2.07	2.69	2.07
Flexural Modulus (x 10^{10} Pa) Warp[2]	1.20	2.07	2.20	2.41	2.89	2.20
Tensile Strength (x 10^8 Pa) Fill[1]	4.13	4.13	4.13	3.93	4.82	3.45
Tensile Strength (x 10^8 Pa) Warp[2]	4.82	4.48	5.24	4.27	5.51	4.13

[1] Fill - yarns that are woven in a crosswise direction of the fabric.
[2] Warp (cloth) - yarns that are woven in the lengthwise direction of the fabric.
[3] Z-axis expansion above T_g can be as much as four times greater. For FR-4 it is 240-390 ppm. Contact supplier for specific values of the other materials.

In actual application, most adhesive needs can be addressed by a few carefully selected materials. Storage and shelf life limitations apply to most of these materials.

4.2.2.1 Epoxies Epoxy resin formulations are among the most versatile adhesives for electrical insulating and mechanical bonding applications. They offer a wide range of physical and electrical properties, including adhesive and cohesive strengths, hardness, chemical resistance, thermal conductivity and thermal vacuum stability. They arealso available with a wide range of cure methods and times. A thorough review of the material is warranted, based on its intended use. Thermal coefficient of expansion and glass transition temperatures should be considered, in addition to other properties, to preclude problems. Epoxies are available with a variety of modifiers, fillers and reinforcements for specific applications and extended temperature ranges.

4.2.2.2 Silicone Elastomers Silicone elastomers are generally noted for being resilient materials with very good electrical and mechanical properties at ambient and extreme temperatures. Several curing methods are available, including moisture, metallic salts and others. Silicone elastomers which evolve acetic acid during their cure should be avoided in electronic applications. Bond strength, tensile strength, and hardness properties tend to be considerably lower than epoxies. Silicones will swell and dissolve with prolonged exposure to some chemicals. Some of the metallic salts curing silicones will react with TFE and PTFE materials. Conformal coatings other than silicones generally will not adhere to cured silicone materials. Silicones are often used as a cushioning overcoat for articles which will be encased in hard potting compounds later.

A number of high purity grades of silicones are available which offer good thermal vacuum stability. Silicone gels are also available, which offer enhanced properties as encapsulants. These materials generally require physical restraint, such as a potting cup or enclosure to maintain their form, once applied.

4.2.2.3 Acrylics Acrylic resins generally provide rapid cures, good electrical and adhesive properties and hardness. Chemical resistance and thermal vacuum stability tend to

be considerably lower than the epoxies. The glass transition temperature of these materials also tends to be low.

4.2.2.4 Polyurethanes Polyurethanes are available in almost as many variations as the epoxies. These materials generally offer toughness, high elasticity, a wide range of hardness, and good adhesion. Some of the urethane compounds are outstanding as vibration and shock damping materials. Moisture and chemical resistance is relatively high, but varies with the individual product. Thermal vacuum stability will also vary by the individual product formulation. Many of the urethanes can be used in a relatively thick application as a local vibration damping compound.

4.2.2.5 Specialized Acrylate-Based Adhesives This category includes the cyanoacrylates (instant cure) and anaerobic adhesives (cure without air). The cyanoacrylates form strong bonds within seconds without catalysts when only a trace amount of moisture is present on a surface. The anaerobic adhesives cure in the absence of oxygen when a peroxide additive can be decomposed by certain transition metal ions. Both adhesive types can give high initial bond strengths which may be beneficial for wire staking and temporary bonding applications. The instant cure adhesives generally have poor impact resistance and are susceptible to degradation from exposure to moisture and temperatures over 82 °C [179.6 °F]. The anaerobic adhesives have the capability of withstanding higher temperatures but can lose strength with prolonged exposure to chemicals.

4.2.2.6 Other Adhesives Many other types and forms of adhesives are available, including polyesters, polyamides, polyimides, rubber resins, vinyl, hot melts, pressure sensitive, etc. Where they are used is determined by the needs of the design and its performance requirements. Selection of specialized items, such as chip bond adhesives, should be done in conjunction with the using facility, in order to ensure full compatibility of the equipment and process.

4.2.3 Adhesive Films or Sheets Adhesive films or sheets used for bonding heatsinks, stiffeners, etc., or as insulators, are generally in accordance with IPC-4203 or IPC-4101.

Film type adhesives find many uses in laminated structures. The ability to pre-cut a film adhesive to fit given shapes or dimensions is a distinct advantage in the fabrication of some laminated parts. Epoxy based film adhesives provide very good bond strength but require elevated temperature cure. Film adhesives are commonly used to bond board heatsinks to printed boards.

Through-hole technology (THT) printed boards and heatsinks may be bonded together with a dry epoxy sheet adhesive to improve heat transfer or resist vibration. These adhesives consist of an epoxy impregnated glass cloth which is cut to the heatsink configuration, assembled between printed board and heatsink, then cured with heat and pressure. The cured adhesive is strong and resists vibration, temperature extremes, and solvents. Thicknesses of 0.1 mm [0.0039 in] should be adequate for most applications. If necessary, specify two sheets.

4.2.4 Electrically Conductive Adhesives This class of adhesives consists, generally, of a conductive filler, such as graphite (carbon) or silver, embedded in a polymeric resin adhesive system, which is loaded into the material to achieve conductivity. Volume resistivity, a measure of the electrically conductive property of the material, may be varied over a range of values consistent with the intended application. This is accomplished by the type of filler used and the loading. Bonding strength of these materials can be compromised by the filler material.

Epoxies, silicone elastomers and urethanes are the resin systems commonly used to formulate conductive adhesives. The strongest bonds are generally achieved with conductive epoxy. Silicone elastomers follow, with urethanes a close third. Cure conditions and filler content have a pronounced effect upon tensile strength of these materials. The choice of conductive adhesive for a particular application should consider the strength of bond, the service temperature, the effect of CTE on the bond and the volume resistivity or conductivity required.

4.2.5 Thermally Conductive/Electrically Insulating Adhesives Thermally conductive adhesives are filled versions of epoxy, silicone, urethane and some acrylic base materials. The filler is normally dried aluminum oxide or magnesium oxide powder.

4.2.5.1 Epoxies The epoxies offer the greatest bond strength and best solvent resistance, along with good thermal conductivity and electrical resistance. As with most two part systems, the choice of catalyst has an impact on cure conditions and ultimately could affect the glass transition temperature, since it is somewhat dependent upon cure conditions.

4.2.5.2 Silicone Elastomers The silicone elastomers are characterized by relatively low bond strengths and less rigidity (lower hardness) than epoxies. They are less resistant to solvent attack than epoxy and are two part systems with other variable properties dependent upon formulation. Thermal conductivity and electrical resistance properties are good.

Silicone elastomers may be obtained as humidity curing or heat curing, the latter offering accelerated cure with applied heat. They cure well in contact with most materials except butyl and chlorinated rubbers, some RTV silicone elastomers and residues of some curing agents. Some bonding applications may require a primer.

4.2.5.3 Urethanes Urethanes can be varied through a wide range of hardness, tensile and electrical properties by varying the proportions of curing agent to resin. Consistency can be varied from a soft, rubbery state to a hard, rigid condition by this method. The latitude for formulation optimization over a range of application conditions is an advantage offered by the filled urethanes.

The urethanes are characterized by relatively low bond strengths and less rigidity (lower hardness) than epoxies. They are less resistant to solvent attack than epoxy; are two part systems with variable other properties dependent upon formulation. Thermal conductivity and electrical resistance properties are good.

4.2.5.4 Use of Structural Adhesives as Thermal Adhesives In design circumstances where thermal conduction properties are not critical, the use of structural adhesives (see 4.2.2) in place of thermal adhesives may be acceptable as determined by thermal analysis and may be a more cost effective alternative.

4.3 Laminate Materials Laminate materials should be selected from material listed in IPC-4101 or IPC-4202. When Underwriter's Labs (UL) requirements are imposed, the material used must be approved by UL for use by the printed board manufacturer.

The board design **shall** be such that internal temperature rise due to current flow in the conductor, when added to all other sources of heat at the conductor/laminate interface, will not result in an operating temperature in excess of that specified for the laminate material or maximum sustained operating temperature of the assembly.

Since heat dissipated by parts mounted on the boards will contribute local heating effects, the material selection **shall** take this factor, plus the equipment's general internal rise temperature, plus the specified operating ambient temperature for the equipment into account for maximum operating temperature.

Hot spot temperatures **shall** not exceed the temperatures specified for the laminate material selected. See IPC-2222 for maximum operating temperature specified for laminate materials. Materials used (copper-clad, prepreg, copper foil, heatsink, etc.) **shall** be specified on the master drawing.

4.3.1 Color Pigmentation Natural colored stock is preferred, because whenever a pigment is added to change a color, the possibility exists for the pigment to retard the ability of the impregnating resin to completely wet each and every glass fiber. Without complete wetting, moisture can be trapped.

Colored stock should not be used because the material usually costs more. Production delays may also be incurred because of lack of availability of the colored stock. If colored stock is required, it **shall** be specified on the procurement documentation.

4.3.2 Dielectric Thickness/Spacing The minimum dielectric thickness/spacing **shall** be specified on the master drawing.

4.4 Conductive Materials The primary function of metallic coatings is to contribute to the formation of the conductive pattern. Beyond this primary function, specific platings offer such additional benefits as corrosion prevention, improved long term solderability, wear resistance, and others.

The thickness and integrity requirements for metallic platings and coatings on as-produced boards **shall** be in accordance with the requirements of Table 4-3 for the appropriate class of equipment. Unless otherwise specified on the master drawing, metallic platings and coatings **shall** meet the requirements specified in 4.4.1 through 4.4.8. Attention should be paid to the effects of dissimilar metals in areas such as connectors, sockets, and other interfaces. The result of a poor material selection could be a reduction in function, either mechanical or electrical.

4.4.1 Electroless Copper Plating Electroless copper is deposited on the surface and through holes of the printed board as a result of processing the drilled panel through a series of chemical solutions. Typically, this is the first step in the plating process and is usually 0.6 µm to 2.5 µm [24 µin to 98.4 µin] thick. Electroless copper can also be used to fully build the required copper thickness, which is referred to as additive plating.

4.4.2 Semiconductive Coatings Semiconductive coatings for direct metallization are used as a conductive starter coating prior to electrolytic copper plating and are applied to the hole wall. The coating should be of sufficient quality for subsequent metallic deposition and **shall** be non-migrating. This process is typically fabricator dependent and is not specified on the master drawing. Palladium and tin are commonly used materials. A thin layer is deposited on exposed surfaces, especially inside drilled holes. This provides a surface for auto-catalyzing the electroless copper deposition.

4.4.3 Electrolytic Copper Plating Electrolytic copper can be deposited from several different electrolytes, including copper fluoroborate, copper cyanide, copper sulfate, and copper pyrophosphate. Copper sulfate and copper pyrophosphate are the most commonly used electrolytes for building the copper deposition on the surface and through the holes to the required thickness. This type of plating usually produces the final copper thickness requirement.

4.4.4 Gold Plating A variety of gold platings are available for depositions on printed boards. These may be electrolytic, electroless, or immersion deposits. The electrolytic

Table 4-3 Final Finish, Surface Plating Coating Thickness Requirements

Code	Finish	Class 1	Class 2	Class 3
S	Solder Coating over Bare Copper	Coverage and Solderable[5]	Coverage and Solderable[5]	Coverage and Solderable[5]
T	Electrodeposited Tin-Lead (fused) (min)	Coverage and Solderable[5]	Coverage and Solderable[5]	Coverage and Solderable[5]
TLU	Electrodeposited Tin-Lead Unfused (min)	8.0 µm [315 µin]	8.0 µm [315 µin]	8.0 µm [315 µin]
G	Gold (min) for edge-board connectors and areas not to be soldered	0.8 µm [31.5 µin]	0.8 µm [31.5 µin]	1.25 µm [49.21 µin]
GS	Gold (max) on areas to be soldered	0.45 µm [17.72 µin]	0.45 µm [17.72 µin]	0.45 µm [17.72 µin]
GWB-1	Gold Electroplate for areas to be wire bonded (ultrasonic) (min)	0.05 µm [1.97 µin]	0.05 µm [1.97 µin]	0.05 µm [1.97 µin]
GWB-2	Gold Electroplate for areas to be wire bonded (thermosonic) (min)	0.3 µm [11.8 µin]	0.3 µm [11.8 µin]	0.8 µm [31.5 µin]
N	Nickel - Electroplate for Edge Board Connectors (min)	2.0 µm [78.7 µin]	2.5 µm [98.4 µin]	2.5 µm [98.4 µin]
NB	Nickel - Electroplate as a barrier to Copper-Tin Diffusion[1] (min)	1.3 µm [51.2 µin]	1.3 µm [51.2 µin]	1.3 µm [51.2 µin]
OSP	Organic Solderability Preservative	Solderable	Solderable	Solderable
ENIG	Electroless Nickel	3 µm [118 µin] (min)	3 µm [118 µin] (min)	3 µm [118 µin] (min)
	Immersion Gold	0.05 µm [1.97 µin] (min)	0.05 µm [1.97 µin] (min)	0.05 µm [1.97 µin] (min)
IS	Immersion Silver	Solderable	Solderable	Solderable
IT	Immersion Tin	Solderable	Solderable	Solderable
C	Bare Copper	As indicated in Table 10-1 and/or Table 10-2		
Surface and Holes				
	Copper[2] (min.avg.)	20 µm [787 µin]	20 µm [787 µin]	25 µm [984 µin]
	Min. thin areas[3]	18 µm [709 µin]	18 µm [709 µin]	20 µm [787 µin]
Blind Vias				
	Copper (min. avg.)	20 µm [787 µin]	20 µm [787 µin]	25 µm [984 µin]
	Min. thin area	18 µm [709 µin]	18 µm [709 µin]	20 µm [787 µin]
Low Aspect Ratio Blind Vias[4]				
	Copper (min. avg.)	12 µm [472 µin]	12 µm [472 µin]	12 µm [472 µin]
	Min. thin area	10 µm [394 µin]	10 µm [394 µin]	10 µm [394 µin]
Buried Via Cores				
	Copper (min. avg.)	13 µm [512 µin]	15 µm [592 µin]	15 µm [592 µin]
	Min. thin area	11 µm [433 µin]	13 µm [512 µin]	13 µm [512 µin]
Buried Vias (> 2 layers)				
	Copper (min. avg.)	20 µm [787 µin]	20 µm [787 µin]	25 µm [984 µin]
	Min. thin area	18 µm [709 µin]	18 µm [709 µin]	20 µm [787 µin]

[1] Nickel plating used under the tin-lead or solder coating for high temperature operating environments act as a barrier to prevent the formation of copper-tin compounds.
[2] Copper plating thickness applies to surface and hole walls.
[3] For Class 3 boards having a drilled hole diameter <0.35 mm [<0.0138 in] and having an aspect ratio >3.5:1, the minimum thin area copper plating in the hole **shall** be 25 µm [984 µin].
[4] Low Aspect Ratio Blind Vias refer to blind vias produced using a controlled depth mechanism (e.g., laser, mechanical, plasma or photo defined). All performance characteristics for plated holes, as defined in this document, **shall** be met.
[5] See also 4.4.7, Solder Coating.

deposition may come in 24k soft gold, 23+k hard gold (hardening uses trace amounts of cobalt, nickel, or iron which are co-deposited with the gold), or the plating may be a lower karat alloy (14k-20k) for some applications. Gold plating serves several purposes:

1. To act as a self lubricating and tarnish resistant contact for edge board connectors (see Table 4-3). Hard electrolytic gold plating is most often used for this application.
2. To prevent oxidation of an underlying plating such as nickel and electroless nickel to enhance solderability

and extend storage life. Electrolytic, immersion and electroless gold are most often used for this purpose (see Table 4-3 for thickness).

3. To provide a wire bonding surface. This application employs a soft 24k electrolytic gold, see Table 4-3 for thickness.
4. To provide an electrically conductive surface on printed wiring boards when electrically conductive adhesives are used. A minimum thickness of 0.25 µm [9.84 µin] is recommended.
5. To act as an etch resist during printed board fabrication, a minimum thickness of 0.13 µm [5.12 µin] is recommended.

Electrolytically deposited gold is often specified as required to meet ASTM-B-488 with the type and grade selected to satisfy the different applications. A low-stress nickel or electroless nickel **shall** be used between the gold overplating and the basis metal when gold finish is to be used for electrical or wire bonding.

Electroless nickel immersion gold plating **shall** be as specified in IPC-4552.

Table 4-4 will help clarify some of the uses for the various alloys.

Table 4-4 Gold Plating Uses

Minimum Purity	Knoop Hardness	Contacts	Wire Bonding	Soldering
99.0	130-200	S	C*	C**
99.0	90 max	NR	S	C**

S - Suitable use NR - Not recommended C - Conditional use
* May be used, but will depend on type of wire bonding being used. Run Test prior to wire bonding.
** More than 0.8 µm [31 µin] gold on boards or leads may cause embrittled solder joints.

4.4.5 Nickel Plating Nickel plating serves a dual function in contact plating: 1) It provides an anvil effect under the gold providing an essential extra hardness to the gold; 2) It is an effective barrier layer (when its thickness exceeds 2.5 µm [98.4 µin]) which prevents the diffusion of copper into gold. This diffusion process can result in a room temperature alloying of the gold, degrading the electrical and corrosion resistance characteristics of the contact.

All electrolytically deposited nickel plating **shall** be low-stress and conform to AMS-QQ-N-290, Class 2, except that the thickness **shall** be as specified in Table 4-3.

Reasons for using a nickel underplate include:

Diffusion Barrier:

- To inhibit diffusion of copper from the basis metal (and of zinc from brass) to the surface of the precious metal plating.
- To inhibit interdiffusion between the basis metal and the gold top coat (for example, silver and copper), which might produce a weak alloy or intermetallic compound at the interface.

Levelling Layer:

- To produce a smoother surface than the basis metal in order to ensure a lower porosity gold top plate (for example, levelling nickel over a rough substrate).

Pore Corrosion Inhibitor:

- A nickel underplate under the gold top coat will form passive oxides at the base of pores in humid air, provided the environment does not contain significant amounts of acidic pollutants (such as SO_2 or HCl).

Tarnish Creepage Inhibitor for Gold:

- Non-copper base metals will inhibit creepage of copper tarnish films over the gold—where the tarnish originates from pores and bare copper edges.

Load-Bearing Underlayer for Contacting Surfaces:

- A hard nickel underplate can serve as a load-bearing foundation for the gold top coat to prevent cracking of hard golds and reduce the wear of the precious metal during sliding of the contacting surfaces. For all these purposes, the nickel underplating must be intact (that is, not cracked) and must have sufficient thickness to achieve the particular function for which it was intended. As a general rule, the minimum thickness should be 1.2 µm [47.2 µin], preferably greater. For some levelling purposes, a far greater thickness may be required.

4.4.6 Tin/Lead Plating Tin/Lead Plating is applied in the subtractive fabrication process to provide a copper etch resist and a solderable coating, when required. Typical thickness sufficient for etch resist on 2 oz. copper is 8.0 µm, but it is a fabrication process parameter, not a design requirement. The electrodeposit is generally fused by one of several techniques (hot oil immersion, infrared exposure, exposure to hot vapors or inert liquids). The fusing operation results in the formation of a true alloy on the surface and in the through holes of the printed board. Fusing is required unless the unfused option is selected to maintain flatness. It also promotes improved long-term solderability.

Tin lead plating does not apply to buried plated-through holes which are internal to the printed board and do not extend to the surface.

Tin-lead plating **shall** meet the composition requirements of ASTM-B-579.

4.4.6.1 Tin Plating Tin Plating is applied in the subtractive fabrication process to provide a copper etch resist.

4.4.7 Solder Coating Solder coating is generally applied by immersing the printed board into molten solder and removing the excess by blowing hot, pressurized air, oil or vapors over the surface of the printed board in a specially designed machine.

Solder coating does not apply to buried or tented plated-through holes which are internal to the printed board and do not extend to the surface.

Unless otherwise specified on the master drawing, the solder used for solder coating **shall** be in accordance with J-STD-006. Solder coating thickness may be specified for particular applications. The performance of solder coating is evaluated, not by a mechanical thickness measurement, but by the ability of the printed board to pass solderability testing per J-STD-003 (see Table 4-3). The user has the responsibility to determine if steam aging, prior to solderability testing, is required.

4.4.8 Other Metallic Coatings for Edgeboard Contacts In addition to the coatings cited previously, there are several other options that the designer may want to consider:

- Rhodium – a low resistance contact coating for flush circuits, switches or where a high number of insertions is expected. Expense has precluded its general use.
- Tin/Nickel Alloy – an abrasion resistant coating.
- Palladium/Nickel Alloy – a low resistance contact coating. May be particularly useful for flush circuits.
- Electroless Nickel and Immersion Gold – a low resistance contact coating suitable for low number of insertions.

4.4.9 Metallic Foil/Film

4.4.9.1 Copper Foil There are two types of copper foil available: (W) – wrought (or rolled), and (ED) – electrodeposited. There are also several copper foil grades. For rigid boards, electrodeposited copper foil is generally used. For flexible boards, wrought foil is generally used. Whichever type is used, the copper foil **shall** conform to the requirements of IPC-4562.

The thickness of starting copper conductors **shall** be as defined in Table 4-5 for the appropriate class of equipment (a reduction in copper thickness of inner layers may be expected after processing). See Appendix A of IPC-4562 for details of foil properties.

4.4.9.2 Copper Film Copper film **shall** be in accordance with Table 4-5.

It should be noted that the minimum material properties for electrodeposited copper foils given in IPC-4562 are inadequate for many printed board designs and applications. This is particularly the case for IPC-4562/1 (CV-E1), IPC-4562/2 (CV-E2), and IPC-4562/3 (CV-E3). While the vast majority of the foil product sold under these slash sheet specifications far exceed the minimum property values, some product sold barely meets these specifications. Thus, it is prudent to obtain actual material properties for critical product.

Table 4-5 Copper Foil/Film Requirements[1]

Copper Type	Class 1-3
Minimum Starting Copper Foil - external	1/8 oz/ft^2 (5 μm) [197 μin]
Minimum Starting[2] Copper Foil - internal	1/4 oz/ft^2 (9 μm) [354 μin]
Starting Copper Film (semi-additive)	5 μm [197 μin]
Final Copper Film (fully-additive)	15-20 μm [591-787 μin]

1. All dimensional values are nominal and derived from weight measurements.
2. 1/8 oz/ft^2 (5 μm) [197 μin] may be used for buried via applications.

4.4.9.3 Other Foils/Film When other foils or films (nickel, aluminum, etc.) are used, their characteristics **shall** be specified on the master drawing.

4.4.9.4 Metal Core Substrates Substrates for metal core boards **shall** be in accordance with Table 4-6.

Table 4-6 Metal Core Substrates

Material	Specification	Alloy
Aluminum	SAE-AMS-QQ-A-250	As specified on master drawing
Steel	QQ-S-635	As specified on master drawing
Copper	ASTM B-152 IPC-4562	As specified on master drawing
Copper-Invar-Copper Copper-Moly-Copper	IPC-CF-152	As specified on master drawing
Other	User defined	As specified on master drawing

4.4.10 Electronic Component Materials

4.4.10.1 Buried Resistors Incorporating buried resistance technology is considerably more expensive than standard multilayer board fabrication. This is due to the special material copper foil purchasing, additional imaging and etching, and resistance (ohm) value verification.

One of the main printed board attributes that requires buried resistance technology is the availability of component real estate. Some high-density designs do not permit discrete resistors. In these cases, buried resistors are viable because they are considerably smaller and when buried allow surface mount components or surface circuitry to pass over them.

An annular resistor is a polymer resistor that can be formed in the empty annulus or "antipad" which surrounds each via hole which passes through the plane or circuit layer. The annular design allows the resistor to be screened with a minimum number of factors which will affect the final resistor value. The primary use of this type of resistor is to replace pull up or pull down resistors that have an acceptable tolerance of ± 10% or greater. This resistor may be produced much less expensively than a surface resistor and

does not require any room on the printed board surface. The larger resistor tolerance and limited number of resistor types that can be replaced are the primary design limitations.

4.4.10.2 Buried Capacitors Distributed capacitance is a design feature which places the power (VCC - voltage common carrier) and ground plane directly facing and in close proximity to each other. A separation of the two planes by 0.1 mm [0.0039 in] or less will produce a sandwich that will provide a low inductance, high capacitance connection to the active devices on the printed board. This fast switching, low current bypass is most useful in high speed digital applications in which the desire to remove surface capacitors or EMI are key considerations. In most designs two power/ground sandwiches are used to replace the existing power and ground plane layers presently in the printed board. In many cases the bypass capacitors 0.1 µF and smaller may be removed from the printed board.

4.5 Organic Protective Coatings

4.5.1 Solder Resist (Solder Mask) Coatings Coatings and markings **shall** be compatible with each other and with all other parts and materials used in the printed board, and the printed board assembly process, including the board preparation/cleaning required prior to their application. IPC-SM-840 assigns determination of this compatibility to the board fabricator and assembler.

The use of solder resist coatings **shall** be in accordance with the requirements of IPC-SM-840. When required, Class 3 boards **shall** use IPC-SM-840, Class H solder resist. When Underwriters Laboratories (UL) requirements are imposed, the coatings used must be approved by UL for use by the printed board manufacturer's process.

When solder resist is used as an electrical insulator the dielectric properties of the coating **shall** be sufficient to maintain electrical integrity. There should be no solder resist in areas of the board that make contact with the board guides.

If the application or design mandates, the minimum and/or maximum solder mask thickness **shall** be specified on the Master Drawing. The minimum thickness specification is required to meet insulation resistance requirements and **shall** be calculated from SM material specifications. The maximum thickness specification is required for component assembly process issues, such as solder paste applications.

Solder resist coating adhesion to melting metal surfaces (solder coating, tin/lead plating, etc.) cannot be assured, as boards are subjected to temperatures that cause redistribution of the melting metals. When solder resist coating is required over melting metal surfaces, the maximum recommended conductor width, where the coating completely covers the conductor, **shall** be 1.3 mm [0.0512 in].

When conductors of melting metal have a width larger than 1.3 mm [0.0512 in], the design of the conductor **shall** provide a relief through the metal to the base laminate substrate. The relief should be at least 6.25 mm^2 [0.001 in^2] in size and located on a grid no greater than 6.35 mm [0.25 in]. When conductor areas of melting metal are to be left uncovered, the design for all class boards **shall** provide that the solder resist **shall** not overlap the melting metal by more than 1.0 mm [0.0394 in].

Design requirements may dictate that via holes are protected from access by processing solutions during soldering, cleaning, etc. When protection is required, the via **shall** be covered (tented) with permanent solder resist, other polymer coverlay material (not conformal coating), or filled with an appropriate polymer in order to prevent access by the processing solutions.

Tenting or filling of vias **shall** be accomplished so that the hole is covered or filled from both sides.

When tenting over vias is used, the maximum finished hole diameter of the vias **shall** be 1.0 mm [0.0394 in] for Class 1 and 2 equipment, and 0.65 mm [0.0256 in] for Class 3 equipment.

For printed board vias with diameters greater than the maximum, tenting **shall** be agreed to between board user and supplier.

The occurance of solder balls at the assembly level may be related to the surface finish of the solder mask, e.g., matte, glossy, etc.

4.5.1.1 Resist Adhesion and Coverage Adhesion between solder resist and laminate and between solder resist and foil **shall** be complete for the total stipulated coverage area. Oxide treatment, double-treated copper, protective chemical treatment, or other adhesion promoter may be used. The use of an adhesion promoter may need user approval.

When circuit designs include unrelieved copper areas greater than 625 mm^2 [0.9688 in^2], the use of a resist adhesion promoter is advisable.

When polymer coatings are required over nonmelting metals, such as copper, the design should provide that conductors not covered by the resist **shall** be protected from oxidation, unless otherwise specified.

4.5.1.2 Resist Clearance Liquid screened coatings require greater clearances (typically 0.4 - 0.5 mm [0.016 - 0.020 in]) than photoimageable resists (typically 0 - 0.13 mm [0 - 0.00512 in]). Clear areas may have to be provided for assembly fiducials.

Data files usually will contain clearances equal to the land. This will allow the board fabricators to adjust the clearance to meet his process capabilities while meeting minimum design clearance requirements specified on the master drawing.

Solder resist-to-land relationship **shall** meet the registration requirements stated on the master drawing.

4.5.2 Conformal Coatings When required, conformal coatings **shall** meet the requirements of IPC-CC-830 and **shall** be specified on the master drawing or master assembly drawing. When UL requirements are imposed, the coatings **shall** be approved by UL for use by the printed board manufacturer. The designer should be cognizant of compatability issues. Conformal coating is an electrical insulation material which conforms to the shape of the circuit board and its components. It is applied for the purpose of improving surface dielectric properties and protecting against the effects in a severe environment. Conformal coatings are not required on surfaces or in areas that have no electrical conductors. Conformal coatings are not normally required on circuit board edges.

4.5.2.1 Conformal Coating Types and Thickness Conformal coating may be any one of the types indicated. The thickness of the conformal coating **shall** be as follows for the type specified, when measured on a flat unencumbered surface:

Type AR - Acrylic Resin	0.03-0.13 mm [0.00118 in-0.00512 in]
Type ER - Epoxy Resin	0.03-0.13 mm [0.00118 in-0.00512 in]
Type UR - Urethane Resin	0.03-0.13 mm [0.00118 in-0.00512 in]
Type SR - Silicone Resin	0.05-0.21 mm [0.00197 in-0.00828 in]
Type XY - Paraxylylene Resin	0.01-0.05 mm [0.000394 in-0.00197 in]

There are three primary chemical categories in use for conformal coating materials: silicone elastomers, organics, and parylene. All three types provide various levels of protection from solvents, moisture, corrosion, arcing, and other environmental factors that can jeopardize the circuit's operational performance (see Table 4-7). Many surface mount technologies cannot perform adequately without the use of a conformal coating due to the tight spacing of leads and land traces.

Conformal coatings may be used in greater thicknesses as shock and vibration dampening agents. This type of application brings with it the risk of mechanical stress to glass and ceramic sealed parts during cold temperature excursions, which may require the use of buffer materials. Heavy build up of conformal coatings under DIPs may also result in mechanical stress of soldered connections during thermal cycling, unless precautions are taken.

4.5.3 Tarnish Protective Coatings Protective coatings may be applied to bare copper on the unassembled board in order to maintain solderability or appearance for extended periods. These coatings may be dispersed during the soldering operation or may require a separate removal process prior to the soldering operation. The coating requirement **shall** be designated on the master drawing.

4.5.3.1 Organic Solderability Protective Coatings OSP coatings are specifically used to protect the unplated copper lands during storage or dual soldering operations for surface mount components. OSP coatings are useful where flatness is required on surface mount lands. The OSP coating must meet solderability requirements. No specific thickness is required, but resistance to tarnishing and retention of solderability after thermal or environmental exposures is required. When OSP coatings are used, solderability retention, their use and storage life requirement criteria **shall** be documented.

4.6 Marking and Legends When specified on the master drawings, boards and assemblies **shall** be marked by appropriate nonconductive inks, labels, etched characters, or other methods. Marking should be used to provide reference designators, part or serial numbers, revision level, orientation or polarization symbols, bar codes, electrostatic discharge (ESD) status, etc.

The marking locations should be such to avoid placing information under components, in hidden locations after assembly or installation, or on conductive surfaces. Marking should not be placed on surfaces covered with melting metals or opaque coatings. Etched markings may affect electrical characteristics such as capacitance.

Whenever practical, fixed format information such as part number, revision level, layer number, and orientation symbols should be incorporated on the artwork master and be considered during printed board layout. Coupons should include this same information. Variable format information, such as serial numbers, fabricator information, date codes, etc., should be placed in an appropriate area utilizing permanent nonconductive, nonnutrient, and high contrast inks, labels, laser scribes, or other means with sufficient durability to survive assembly and cleaning.

Markings **shall** be of sufficient size, clarity, and location to allow legibility during the processing, inspection, storage, installation, and field repair of a board or assembly. Usually, a minimum character height of 1.5 mm [0.0591 in] with a line width of 0.3 mm [0.012 in] is adequate.

Every attempt should be made to provide enough space for the marking and it is recommended that space be reserved when component placement is determined per 8.1. Avoid

Table 4-7 Conformal Coating Functionality

Type	Advantages	Disadvantages
Silicone elastomers	Resistant to extreme temperature cycling. Good intermittent solvent splash resistance. Low modulus, easily removed, flexible. Works well over most solder resists and no clean fluxes. Easily reworked.	Low mechanical abrasion resistance. Half the dielectric strength of organics. Can impair solderability after coating.
Organics	High dielectric strength. Excellent mechanical abrasion resistance. Excellent solvent resistance. Excellent moisture resistance.	Can only be used to 125 °C [257 °F]. Difficulty of rework varies. Coefficient of thermal expansion needs to be matched. Required compatibility check with solder resist. Required compatibility check with flux chemistry.
Parylene	Extremely high dielectric strength. Excellent conformability around parts. Excellent penetration of polymer. Excellent moisture/chemical resistance.	High raw material cost. Applied in a vacuum chamber (batch process). Masking seals must be air-tight. Thin film leakage difficult to visually detect.

the use of marking inks in close proximity to surfaces that must be solderable as the resin systems used in these inks may impair solderability.

Liquid screened markings require clearances that are typically 0.4 - 0.5 mm [0.016 - 0.020 in] from solderable surfaces. Caution should be used when calling for liquid screened markings. Their legibility is affected by high surface irregularities.

ESD or Underwriters Laboratories requirements may include special marking considerations which **shall** become a part of the master drawing.

4.6.1 ESD Considerations Completed circuit card assemblies **shall** be marked in accordance with the assembly drawing with their full identification. Circuit card assemblies which contain electrostatic discharge sensitive devices **shall** be marked in accordance with EIA Standard RS-471.

The marking **shall** be etched or applied by the use of a permanent ink or a permanent label which will withstand assembly processing and remain visible just prior to removal of the assembly for maintenance. Additional markings, if required, **shall** be specified on the assembly drawing.

5 MECHANICAL/PHYSICAL PROPERTIES

5.1 Fabrication Considerations Table 5-1 lists some fabrication assumptions and considerations.

5.1.1 Bare Board Fabrication Due to the equipment involved in printed board fabrication, there are certain limits that should be taken into account in order to maximize manufacturability and, thereby, minimize costs. Also human factors, such as strength, reach and control, preclude the use of full-size panels in most printed board manufacturing facilities.

5.2 Product/Board Configuration The physical parameters of the printed board should be consistent with the mechanical requirements of the electronic system. Tolerances, as defined in Sections 3 and 5, should be optimized to provide the best fit between the board size, shape, and thickness and mechanical hardware used to mount the product.

5.2.1 Board Type The decision for board type (single-sided, double-sided, multilayer, metal core, etc.) should be made prior to starting layout procedures and be based on assembly performance requirements, heat dissipation, mechanical rigidity requirements, electrical performance (shielding, impedance matching, etc.) and anticipated circuit density (see 3.6.2).

5.2.2 Board Size Boards should be of uniform size whenever possible to facilitate bare board and assembly test fixturing, and minimize the number of fixtures required. An example of board standardization is shown in Figure 5-1. The board size should also be compatible with standard manufacturing panel sizes in order to achieve lowest cost and maximum number of boards per panel. This will also help facilitate bare board testing (see IPC-D-322).

5.2.3 Board Geometries (Size and Shape)

5.2.3.1 Material Size The largest size for a printed board fabrication panel is a function of the economic use of sheet laminate common to the marketplace (see IPC-D-322).

The use of a panel size smaller than the largest sub-multiple of the full-size sheet is recommended. One common panel size is 460 mm x 610 mm [18.110 in x 24.02 in]. Secondary standard panel sizes should be sub-multiples of the full-size sheet.

It is recommended that the designer be aware of the printed board manufacturer's process panel size in order to optimize the board-to-panel yield, and cost relationships. The use of the larger panel sizes is typically the most effective from a labor cost per unit area of end-product board processed. However, the use of large panels may pose difficulties in achieving fine lines and feature positional accuracy due to an increase in base material movement.

Table 5-1 Fabrication Considerations

Fabrication Design Assumptions	Benefits(★), Drawbacks(⇓), Impacts of Not Following Assumptions(⊗), Other Comments(♲)
Hole/Land Ratio: Land size at least 0.6 mm [0.024 in] greater than the hole size[1]	★Provides sufficient land area to prevent breakout, i.e., hole intersecting edge of land (insufficient annular ring) ⇓ Large lands may interfere with minimum spacing
Teardrop at Connection of Run with Land	★Provides additional area to prevent breakout. ★May improve reliability by preventing cracking at land/run boundary in vibration or thermal cycling. ⇓ May interfere with minimum space requirements
Board Thickness: 0.8 mm to 2.4 mm [0.031 in to 0.0945 in] typical (over copper)	⊗Thinner boards tend to warp & require extra handling with through-hole technology components. Thicker boards have lower yield because of layer to layer registration. Some components may not have long enough leads for thicker boards.
Board Thickness to Plated Hole Diameter: Ratios ≤ 5:1 are preferred[1]	★Smaller ratios result in more uniform plating in hole, easier cleaning of holes and less drill wander. ★Larger holes are less susceptible to barrel cracking.
Symmetry across Board Thickness: top half should be a mirror image of bottom half to achieve a balanced construction	⊗Asymmetrical boards tend to warp. ♲The location of ground/power planes, the orientation of signal runs and the direction of the fabric weave affect board symmetry. ⇓ Heavy copper areas should be distributed throughout the area of the board as well to minimize warp.
Board Size	★Smaller boards warp less and have better layer to layer registration. ⇓ Foil lamination or floating layer lay-ups should be considered for large panels with small features ♲Panel utilization determines cost.
Conductor Spacing: ≤0.1 mm [≤0.0039 in]	⊗Etchant fluid does not circulate efficiently in narrower spaces resulting in incomplete metal removal.
Circuit Feature (Conductor Width): ≤0.1 mm [≤0.0039 in]	⊗Smaller features are more susceptible to breakage and damage during etching.

[1] These fabrication considerations, although valuable, may not be practical for some vias. Those vias which have small pad diameters cannot have 0.6 mm [0.024 in] of land size larger than the hole as this violates the board thickness to plated hole (aspect ratio) recommendation. When geometry considerations require small pads, the aspect ratio issue becomes paramount and the annular ring issue should be handled by exception.

5.2.4 Bow and Twist Proper board design, with respect to balanced circuitry construction distribution and component placement, is important to minimize the degree of bow and twist of the printed board. Additionally, the cross-sectional layout, which includes core thicknesses, dielectric thicknesses, inner layer planes, and individual copper layer thicknesses, should be kept as symmetrical as possible about the center of the board.

Unless otherwise specified on the master drawing, the maximum bow and twist **shall** be 0.75% for boards that use surface mount components and 1.5% for all other board technologies. Panels that contain multiple printed boards to be assembled on the panel and later separated **shall** also meet these bow and twist requirements.

If symmetrical construction and tighter tolerances are not sufficient to meet critical assembly or performance requirements, stiffeners or other support hardware may be necessary.

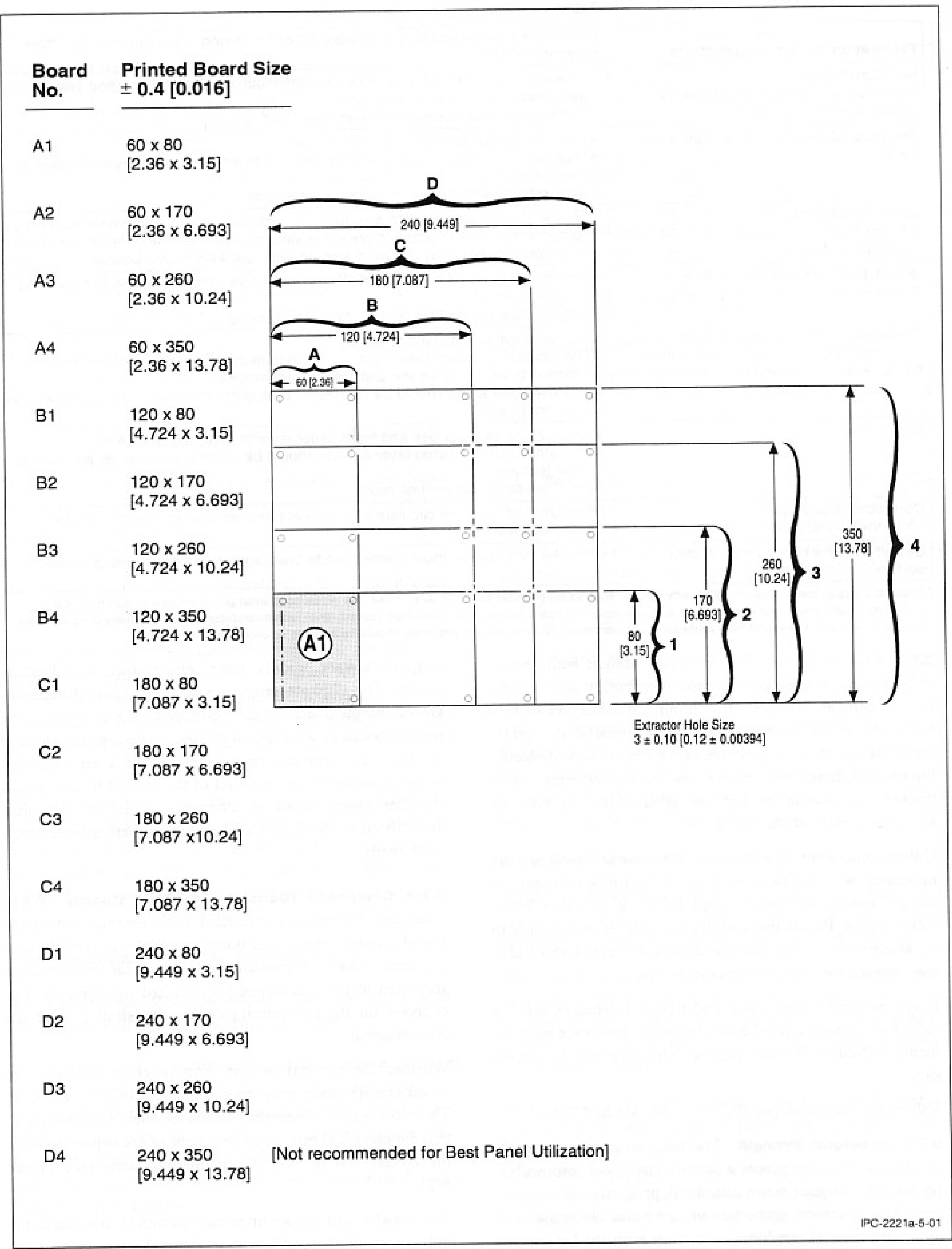
Values are measured per IPC-TM-650, Method 2.4.22.

5.2.5 Structural Strength The wide variety of materials and resins available places a serious analytical responsibility on the designer when structural properties are important. The structural properties of laminates are influenced by environmental conditions that vary with the lay-up and composition of the base materials. Physical and electrical properties vary widely over temperature and loading ranges. The ultimate properties of printed board materials are of marginal use to the designer trying to employ the printed board as a structural member. The concern to meet electrical performance requirements, which are impacted by deformation and elongation of the printed board, should consider lower values of ultimate material strength than those listed in the technical literature for determining structural needs.

5.2.6 Composite (Constraining-Core) Boards When structural, thermal, or electrical requirements dictate the use of a constraining-core board, the physical performance properties **shall** be evaluated using similar conformance specimen to those designed for standard rigid boards. The coupons for the constraining-core board **shall** include the core material.

Whether for thermal or constraining characteristics, the board configuration may be symmetrical or asymmetrical. There are some advantages in an asymmetrical design in that the electrical properties or functions are separated from the mechanical or heat dissipation functions (see Figure 5-2).

The drawback of the asymmetrical design is that due to the differences of the coefficient of thermal expansion of the printed board and the core material, the completed board



Board No.	Printed Board Size ± 0.4 [0.016]
A1	60 x 80 [2.36 x 3.15]
A2	60 x 170 [2.36 x 6.693]
A3	60 x 260 [2.36 x 10.24]
A4	60 x 350 [2.36 x 13.78]
B1	120 x 80 [4.724 x 3.15]
B2	120 x 170 [4.724 x 6.693]
B3	120 x 260 [4.724 x 10.24]
B4	120 x 350 [4.724 x 13.78]
C1	180 x 80 [7.087 x 3.15]
C2	180 x 170 [7.087 x 6.693]
C3	180 x 260 [7.087 x10.24]
C4	180 x 350 [7.087 x 13.78]
D1	240 x 80 [9.449 x 3.15]
D2	240 x 170 [9.449 x 6.693]
D3	240 x 260 [9.449 x 10.24]
D4	240 x 350 [9.449 x 13.78] [Not recommended for Best Panel Utilization]

Figure 5-1 Example of Printed Board Size Standardization, mm [in]

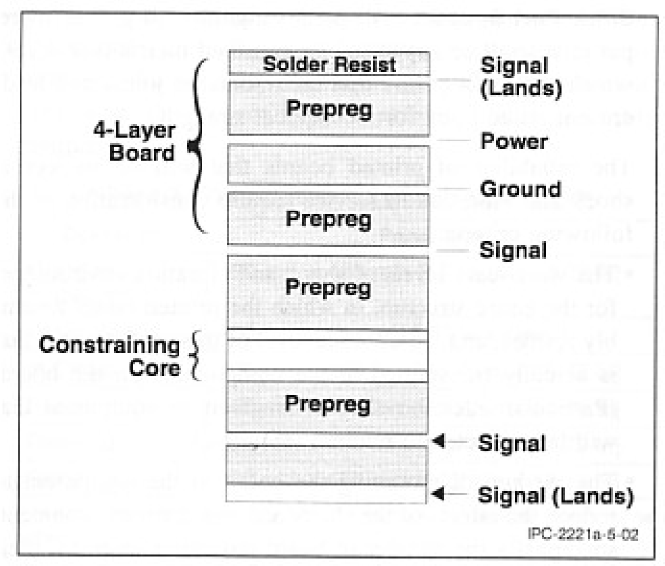


Figure 5-2 Typical Asymmetrical Constraining-Core Configuration

may distort during assembly soldering/reflow operations or while in system use due to temperature change. Some compensation can be achieved by having an additional copper plane added to the back of the interconnection product. The extra copper plane increases the expansion coefficient slightly, but a positive effect is that it enhances thermal conductivity.

A more desirable construction may be that of the symmetrical cored board (see Figure 5-3A and 5-3B). Figure 5-3A shows the two restraining cores laminated into the multilayer board where they serve as part of the electrical function, in this case, power and ground. The center core construction as shown in Figure 5-3B has a single thicker restraining core which usually has only the thermal plane and restraining function. To achieve restraint in the usable range, the combined thickness of the copper-Invar-copper in the multilayer board should be approximately 25% of the board thickness. The two-restraining-core board is more often used because the core layers may be imaged, etched and connected to the plated through hole; the thicker center core must be machined. Better thermal cycle survival is exhibited by the two-restraining-core board.

A special constraining-core board may be made by bonding a multilayer printed board to each side of a thick constraining metal core after the boards have been completed. A more complex variation may also be fabricated wherein the constraining metal core is laminated between two partially completed multilayer printed boards. The composite board is then sequentially drilled, plated and etched to form plated-through hole connections between the two boards. Coupons should be provided to test the integrity of the composite structure.

Metal core boards add significantly to the thermal mass of the assembly. This may force the preheating and soldering process to be operated at abnormally high limits. These

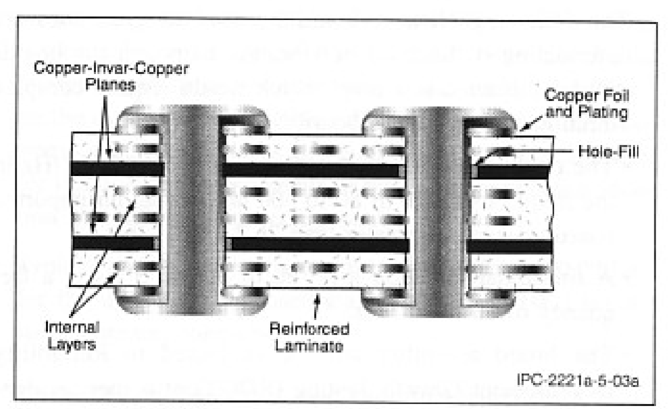


Figure 5-3A Multilayer Metal Core Board with Two Symmetrical Copper-Invar-Copper Constraining Cores (when the Copper-Invar-Copper planes are connected to the plated-through hole, use thermal relief per Figure 9-4)

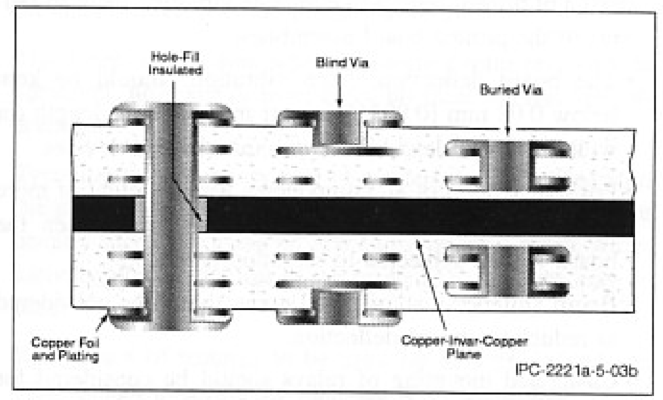


Figure 5-3B Symmetrical Constraining Core Board with a Copper-Invar-Copper Center Core

designs should be thoroughly evaluated under production conditions prior to release. Laminate ruptures and discoloration and grainy or textured solder are typical effects that have been observed.

5.2.7 Vibration Design The design of printed boards that will be subjected to vibration while in service requires that special consideration be given to the board prior to board layout. The effect on the board assembly caused by the vibration can seriously reduce the reliability of the assembly. The interrelationship between the unit, printed board assemblies, their mounting and the environmental conditions make necessary the need for a vibration analysis of the complete system very early in the design. The effect from vibration on any item within a unit can make the vibration analysis very complex.

Vibration analysis should be done on each piece of electronic hardware which contains printed board assemblies. The complexity of the analysis should depend on the vibration level to which the hardware will be subjected in service. The design of the printed boards will depend on the level of vibration transmitted to the board. Particular attention should be given to printed boards subjected to random vibration.

The following criteria should be used as guidelines for determining if the level of vibration to which the boards will be subjected is a level which would require complex vibration analysis of the board:

- The random spectral density is at, or above, $0.1G^2/Hz$ in the frequency range of 80 to 500 hertz or an unsupported board distance of greater than 76.2 mm [3 in].
- A sinusoidal vibration level at, or above, 3 Gs at a frequency of 80 to 500 Hz.
- The board assembly will be subjected to Reliability Development Growth Testing (RDGT) at a spectral density at, or above, 0.07 G^2/Hz for more than 100 hours in conjunction with temperature cycling.

The following guidelines should be observed during the design of printed boards to eliminate vibration induced failures of the printed board assemblies:

- The board deflection, from vibration, should be kept below 0.08 mm [0.00315 in] per mm of board length (or width) to avoid lead failure on multiple lead devices.
- Positive support of all components with a weight of more than 5.0 gm per lead should be considered when the board will be subjected to vibration (see 5.3.2).
- Board stiffeners and/or metal cores should be considered to reduce the board deflection.
- Cushioned mounting of relays should be considered for their usage in high level vibration environments.
- Vibration isolators should be considered for mounting of units whenever practical.
- The mounting height of freestanding components should be kept to a minimum.
- Nonaxial leaded components should be side-mounted.

Because of the interrelationship of the many components that make up a system, the use of the above guidelines does not ensure the success of a unit subjected to a vibration test. A vibration test of a unit is the only way to ensure that a unit will be reliable in service.

5.3 Assembly Requirements

5.3.1 Mechanical Hardware Attachment The printed board **shall** be designed in such a manner that mechanical hardware can be easily attached, either prior to the main component mounting effort, or subsequently. Sufficient physical and electrical clearance should be provided for all mechanical hardware that requires electrical isolation. In general, mounting hardware should protrude no more than 6.4 mm [0.252 in] below the board surface to allow sufficient clearances for assembly equipment and solder nozzles.

5.3.2 Part Support All parts weighing 5.0 gm, or more, per lead **shall** be supported by specified means (see 8.1.9), which will help ensure that their soldered joints and leads are not relied upon for mechanical strength.

The reliability of printed boards that will be subject to shock and vibration in service require consideration of the following criteria:

- The worst-case levels of shock and vibration environment for the entire structure in which the printed board assembly resides, and the ultimate level of this environment that is actually transmitted to the components on the board. (Particular attention should be given to equipment that will be subjected to random vibration.)
- The method of mounting the board in the equipment to reduce the effects of the shock and vibration environment, specifically the number of board mounting supports, their interval, and their complexity.
- The attention given to the mechanical design of the board, specifically its size, shape, type of material, material thickness, and the degree of resistance to bowing and flexing that the design provides.
- The shape, mass and location of the components mounted on the board.
- The component lead wire stress relief design as provided by its package, lead spacing, lead bending, or a combination of these, plus the addition of restraining devices.
- The attention paid to workmanship during board assembly, so as to ensure that component leads are properly bent, not nicked, and that the components are installed in a manner that tends to minimize component movement.
- Conformal coating may also be used to reduce the effect of shock and vibration on the board assembly (see 4.5.2).

Where circuit design permits, the selection of components to be mounted on boards subjected to severe shock and vibration should favor the use of components that are lightweight, have low profiles and inherent strain-relief provisions. Where discrete components must be used, preference should be given to surface mount and/or axially-leaded types that present a relatively low profile that can be mounted and easily clamped or bonded in intimate contact with the board surface.

The use of irregularly-shaped components, especially those having a large mass and a high center of gravity, should be avoided where practical. If their use cannot be avoided, they should be located toward the outer perimeter of the board, or where hardware or mounting reduces flexing. Depending on the severity of this problem, the use of mechanical clamping, adhesive bonding, or embedding may be required.

5.3.3 Assembly and Test Consideration, similar to that mentioned above for printed board fabrication, must be

given to printed board assembly and test equipment utilization in order to improve manufacturing yields and to minimize end-product costs. Table 5-2 provides limits associated with the use of typical printed board assembly equipment.

Table 5-2 Typical Assembly Equipment Limits

Operation	Panel Size
Component Placement	450 mm x 450 mm [17.72 in x 17.72 in]
Wave Solder	400 mm x Open [15.75 in x Open]
In-Circuit Test*	400 mm x 400 mm [15.75 in x 15.75 in]
Reflow	450 mm x 610 mm [17.72 in x 24.02 in]
Cleaning	450 mm x 450 mm [17.72 in x 17.72 in]
Stencil	450 mm x 450 mm [17.72 in x 17.72 in]

*Maximum size also determined by the number of electrical nodes to be tested.

5.4 Dimensioning Systems

5.4.1 Dimensions and Tolerances Historically, printed board designs have used bilateral tolerances for size and position, which is acceptable. However, the use of Geometric Dimensioning and Tolerancing (GDAT) per IPC-2615, has many advantages over bilateral tolerancing:

a) It allows at least 57% more tolerance area with true positioning than with bilateral tolerancing (see Figure 5-4).

b) It provides for maximum producibility while assuring the mechanical function of the printed board. It allows "bonus" or extra tolerances when the maximum/least material concept is used.

c) It ensures that design requirements, as they relate to fit and function, are specifically stated and carried out. This is particularly significant when automated assembly techniques are to be used.

d) It ensures interchangeability of mating parts.

e) It provides uniformity and convenience in drawing delineation and interpretation, thus reducing controversy and guesswork.

For these reasons, the use of geometric dimensioning and tolerancing is encouraged.

5.4.2 Component and Feature Location Grid systems are described in IPC-1902/IEC 60097. Grid systems are used to locate components, plated-through holes, conductor patterns, and other features of the printed board and its assembly so they need not be individually dimensioned. When printed board features are required to be off grid, they may be individually dimensioned and toleranced on the master drawing.

The use of electronic media precludes the necessity for individual component dimensioning.

Grid systems are always basic and have no tolerance, and therefore all features located on a grid **shall** be toleranced on the master drawing. Grid systems shall be located with respect to a minimum of two datums. The selected grid increment or the use of electronic media **shall** be specified on the master drawing. Either the selected grid or the electronic media establishes the component terminal location for through-hole components or the component center location for surface mount components.

Typical grid increments are multiples of 0.5 mm [0.020 in] for through-hole components and 0.05 mm [0.002 in] for surface mount components.

5.4.3 Datum Features Datums are theoretically exact points, axes, and planes. These elements exist within a framework of three mutually perpendicular intersecting planes known as the datum reference frame. Datum features are chosen to position the printed board in relation to the datum reference frame (see Figure 5-4A).

There are some cases where a single datum reference is sufficient, however in most cases all three datums are referenced.

Typically the secondary side of the board is identified with the primary datum. The other two datum planes or axes are usually identified using adjacent unsupported holes. Alternatively, etched features or the printed board edges may be used.

The choice of features to be used for datums depends on what design elements are intended to be controlled. Board edge datums may be used when they represent a major function of the printed board. Datum features **shall** be identified on the master drawing by means of symbols per IPC-2615. Datum features should be functional features of the printed board and should relate to mating parts such as mounting holes. All datum features should be located within the printed board profile. The second datum feature typically becomes the coordinate zero for measurements. It is preferred that this be located within the printed board.

Note: When boards are very dense with circuitry or are very small, there may be no room to have the tooling features located on the board. In these instances the zero-zero origin is off the board and a secondary location is identified for visual orientation. Often times marking ink provides this function.

With the use of electronic data, all holes, conductors and features are viable elements to allow for fabrication and inspection. However, for any feature not dimensioned digitally within the database, it is necessary to delineate dimensions to the design not in electronic format. Some of these characteristics are as follows:

A) Plated Through-Hole Patterns The plated through-hole pattern (see Figure 5-5A) is generally accomplished during the first drilling operation. It can be dimensioned as a basic dimension with each hole toleranced to a basic

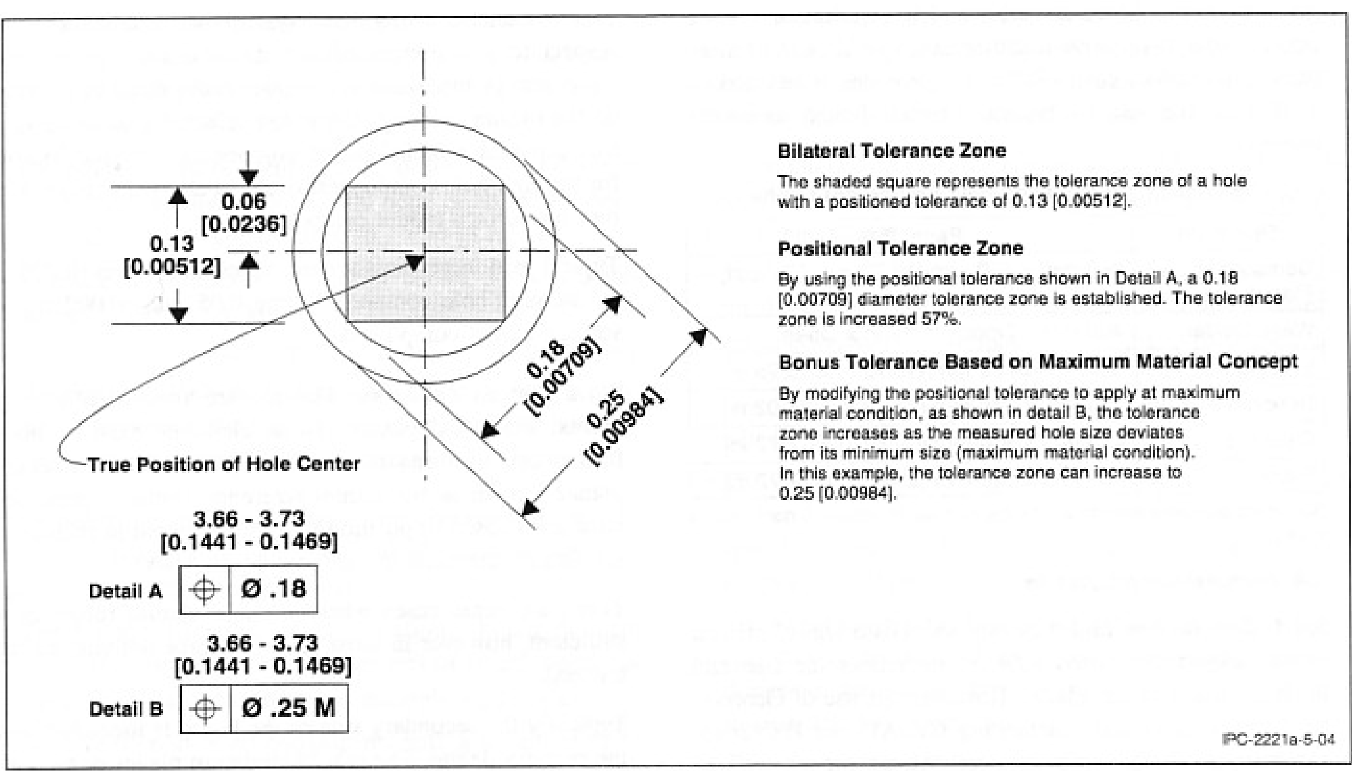


Figure 5-4 Advantages of Positional Tolerance Over Bilateral Tolerance, mm [in]

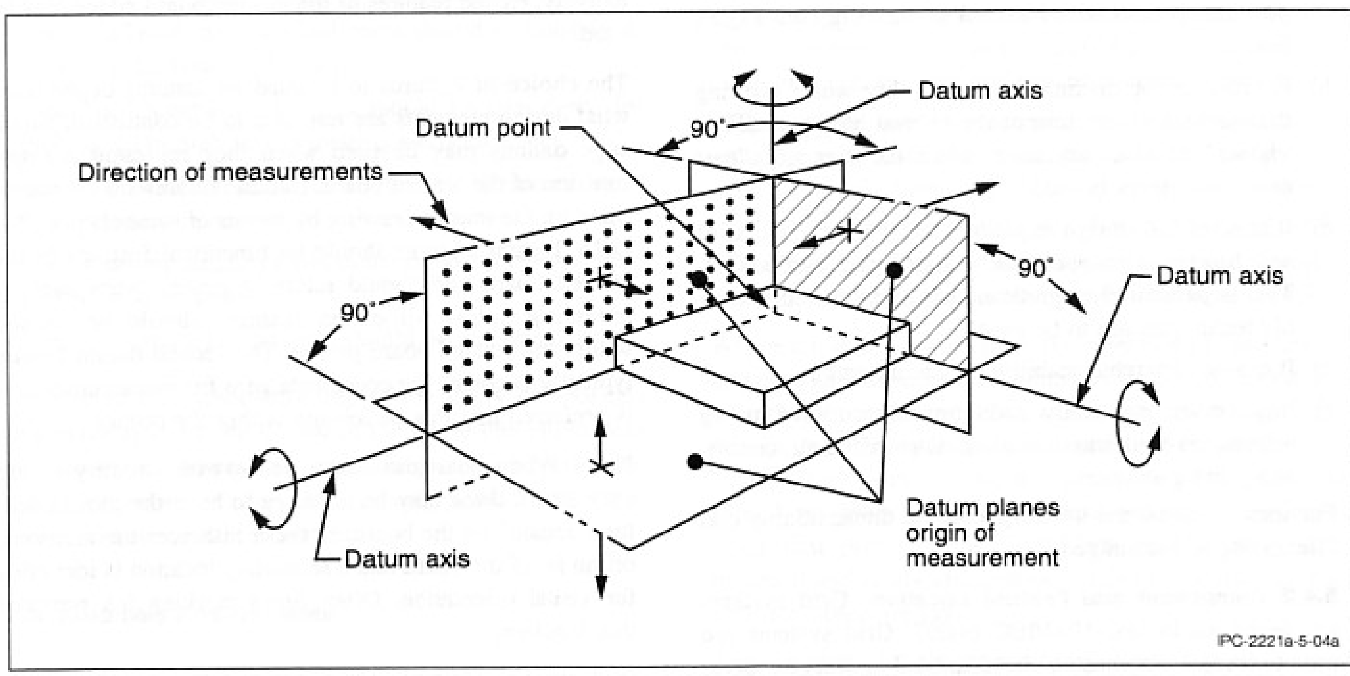


Figure 5-4A Datum Reference Frame

grid location. The hole location tolerance is specified either in the hole list or is best defined by a note on the master drawing.

B) Unsupported Through Hole Patterns Nonplated through-hole patterns, especially tooling and mounting holes (see Figure 5-5B), are generally drilled during the primary drilling operation. They should be explicitly dimensioned and toleranced, even if they occur on grid, when they are critical to boards mounting functionality or the tooling features. Two of these may be identified as datum features for the secondary and tertiary datums.

Tooling holes are features of the printed board or the printed board panel. They are features in the form of a hole that may also be used by board manufacturers to optimize the tolerance conditions between pins on the tooling fixture and the holes or slots in the board.

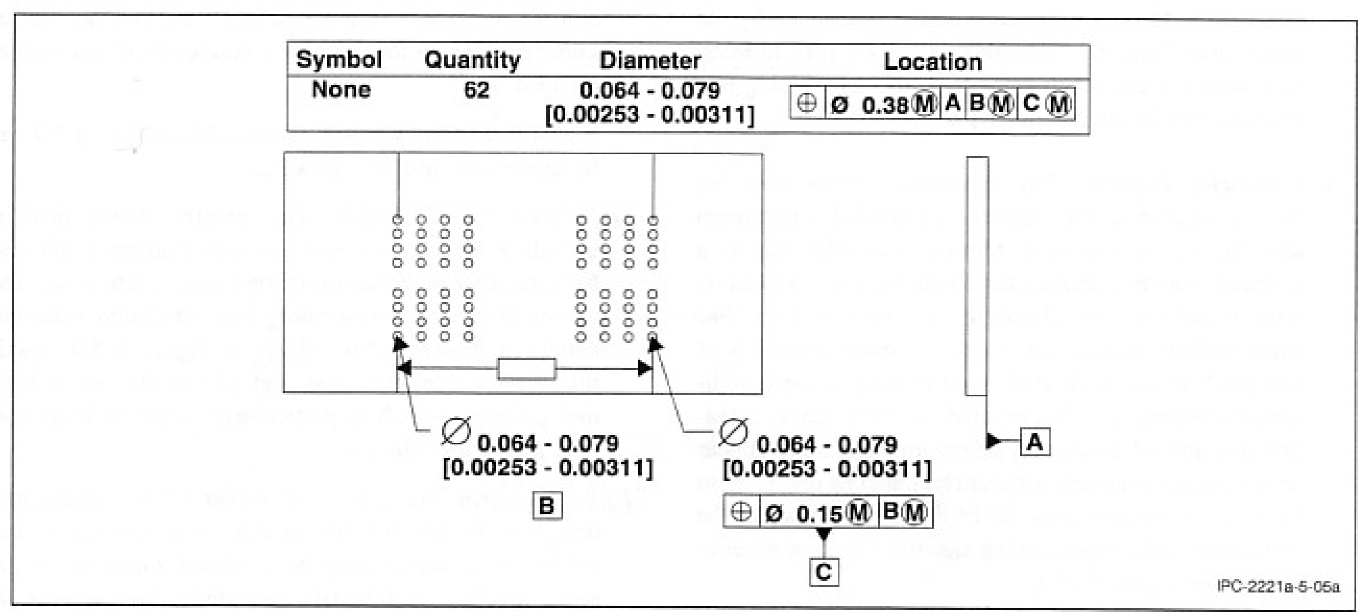


Figure 5-5A Example of Location of a Pattern of Plated-Through Holes, mm [in]

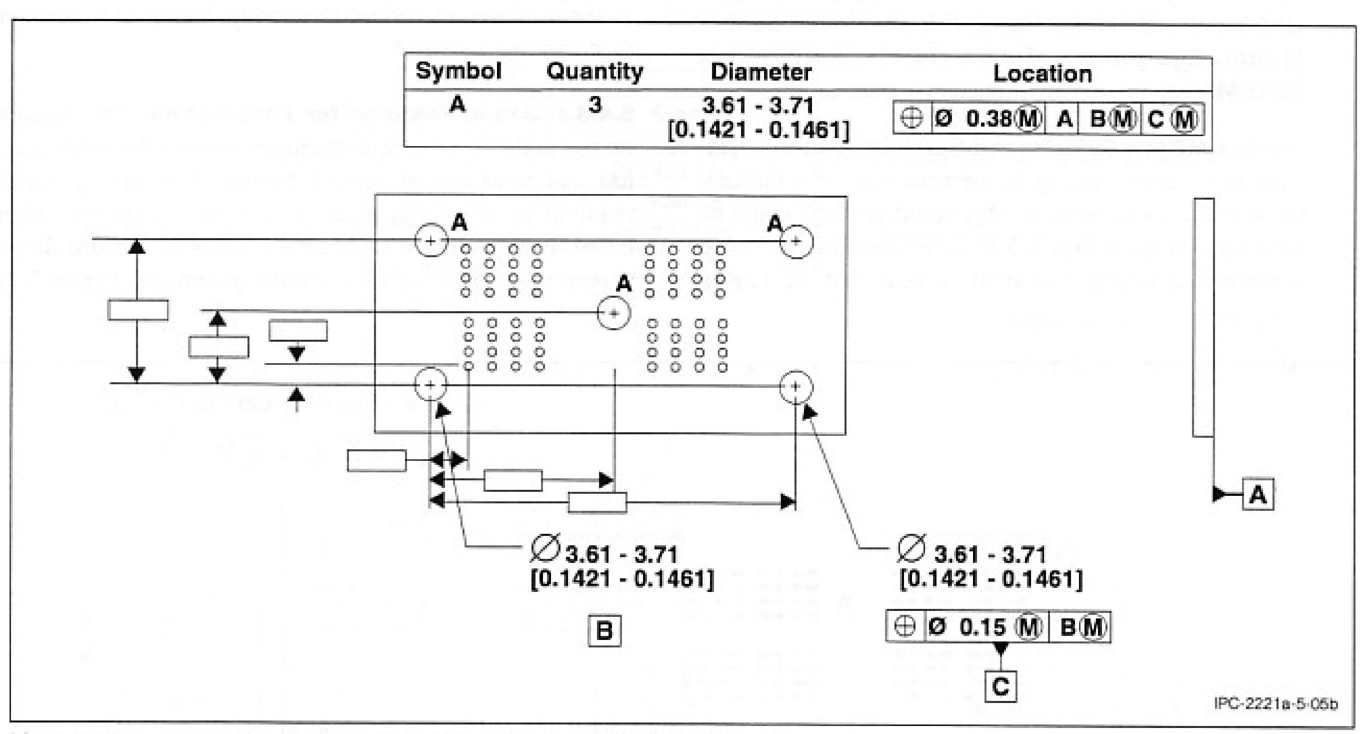


Figure 5-5B Example of a Pattern of Tooling/Mounting Holes, mm [in]

Fabrication tooling holes are usually determined by the board manufacturer, although it is a good plan to interface with the assembler since they also use tooling features as part of the assembly panel.

C) Conductor Patterns The conductor pattern does not need a separate datum reference, provided a minimum annular ring is specified. Minimum annular ring is a common way to tolerance the conductor pattern location with respect to the plated through-hole pattern. For some designs, particularly where automated assembly of fine pitch and/or high lead count devices is used, additional accuracy may be required. In these cases, a feature location tolerance may be required and **shall** appear on the master drawing. Alternately, fiducials restricted to component features may be required. These would be toleranced with respect to the assembly tooling requirements (see Figure 5-5C).

The fiducial size, shape and quantity may depend on the type of equipment used in the assembly process and the lead pitch and count. Figure 5-6 shows the Surface Mount Equipment Manufacturers Association (SMEMA) recommended fiducial design.

Another method to locate and tolerance conductor patterns is by dimensioning to the centerline of a conductor. A critical area such as edge board contacts could be dimensioned as in Figure 5-8. Tolerances used for edge contacts and keying lots **shall** be such that the keying slot does not cut into or damage the contact finger. Dimensioning to the edge of a conductor is not recommended.

Figure 5-5E shows how Figures 5-5A through 5-5D can be assembled into one drawing.

D) Printed Board Profile The printed board profile, including cutouts and notches (see Figures 5-5D and 5-7), requires a minimum of one datum reference. The use of three datum references and maximum material-condition modifiers, as shown in Figure 5-5D, maximizes allowable tolerances and allows the use of hard tool gauging, which is particularly useful in high volume production situations.

E) Solder Resist Coatings The solder resist coating pattern may be located by specifying a minimum land clearance or targets may be provided which serve the same function as fiducials for conductive patterns. A minimum land clearance serves the same purpose as a minimum annular ring requirement in that it tolerances the solder resist pattern location with respect to the conductor pattern.

5.4.3.1 Datum Features for Palletization Palletization or assembly arrays are a common process for facilitating test and assembly of printed boards. A datum system is required for the pallet or array as well as each individual board. It is important to relate the individual board datum system to the pallet or array datum system (see Figure 5-7).

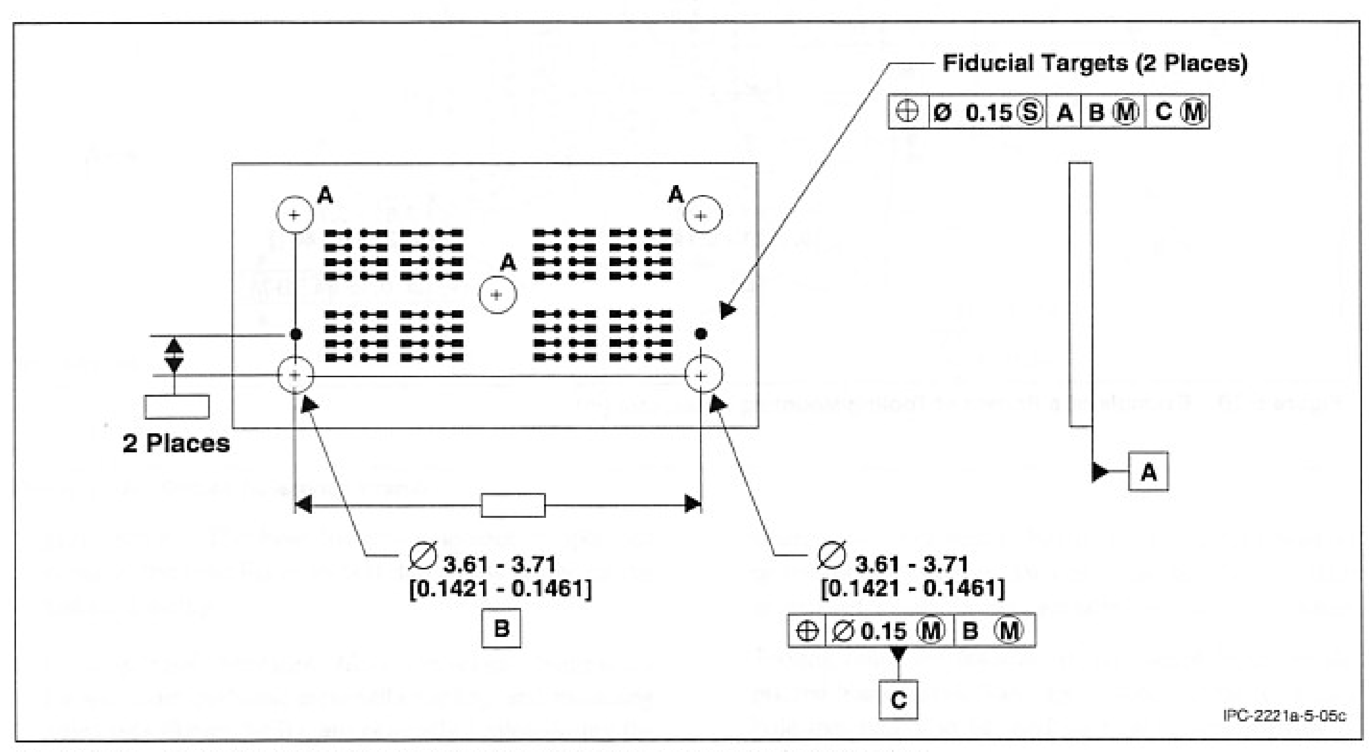


Figure 5-5C Example of Location of a Conductor Pattern Using Fiducials, mm [in]

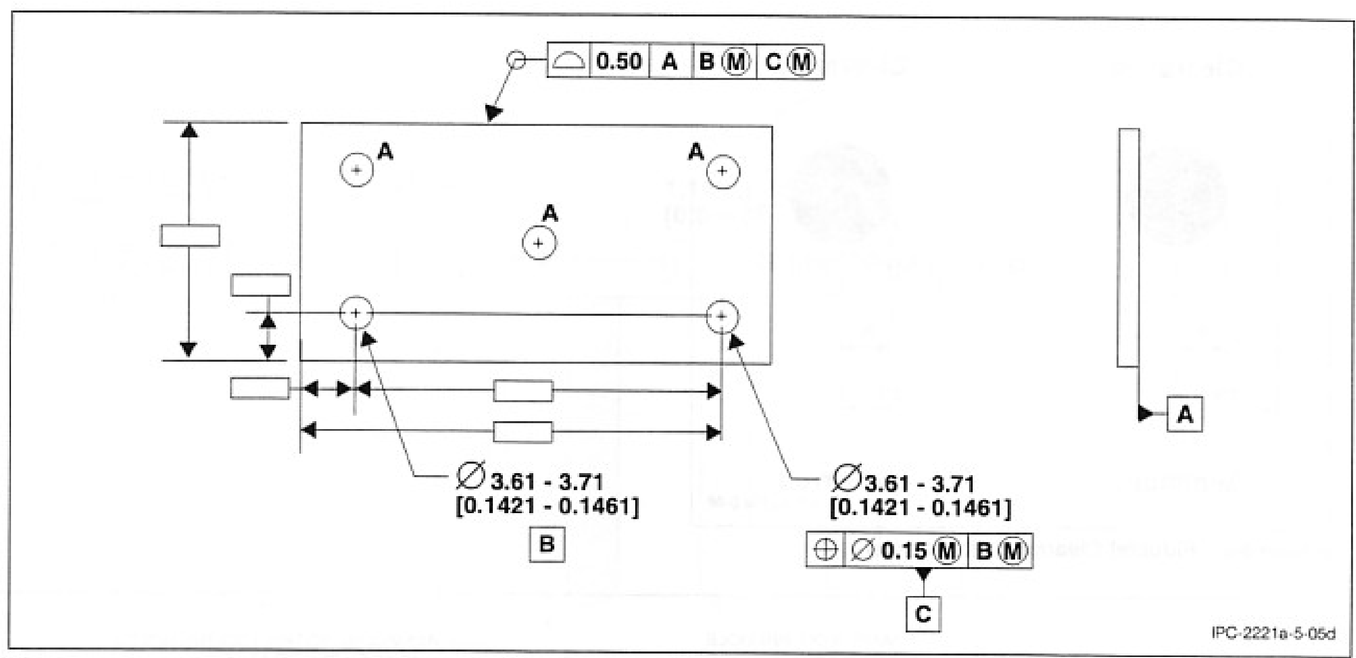


Figure 5-5D Example of Printed Board Profile Location and Tolerance, mm [in]

Symbol	Quantity	Diameter	Location
A	3	3.61 - 3.71 [0.1421 - 0.1461]	Ø 0.38 (M) | A | B (M) | C (M)
None	64	3.64 - 3.79 [0.1433 - 0.1492]	Ø 0.15 (M) | A | B (M) | C (M)

Fiducial Targets (2 Places)

Ø 0.15 | A | B (M) | C (M)

0.5 | A | B (M) | C (M)

A

A

A

2 Places

∅3.61 - 3.71
[0.1421 - 0.1461]

B

∅3.61 - 3.71
[0.1421 - 0.1461]

Ø 0.15 (M) | B (M)

C

A

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Figure 5-5E Example of a Printed Board Drawing Utilizing Geometric Dimensioning and Tolerancing, mm [in]

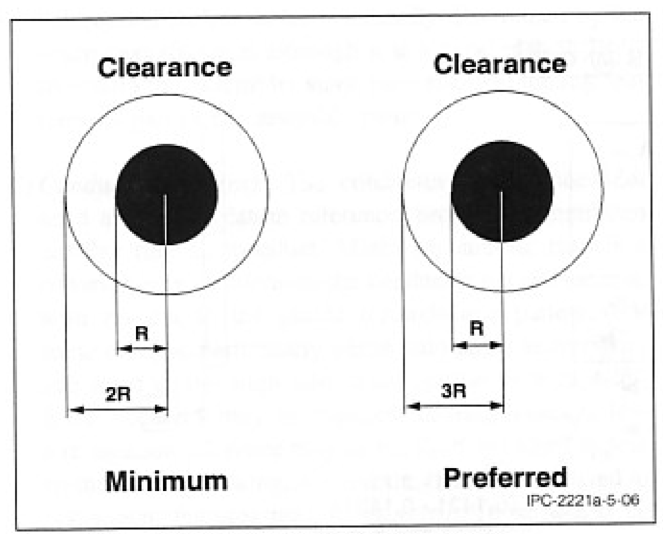


Figure 5-6 Fiducial Clearance Requirements

PANEL TOOLING HOLE
(3 PLACES)

INDIVIDUAL BOARD TOOLING HOLES
(3 PLACES PER BOARD)

X.XXX

X.XXX

X.XXX

X.XXX

X.XX

DATUM

X.XXX

X.XXX

DATUM

X.XX

X.XX

8 BOARD PANELIZATION

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Figure 5-7 Fiducials, mm

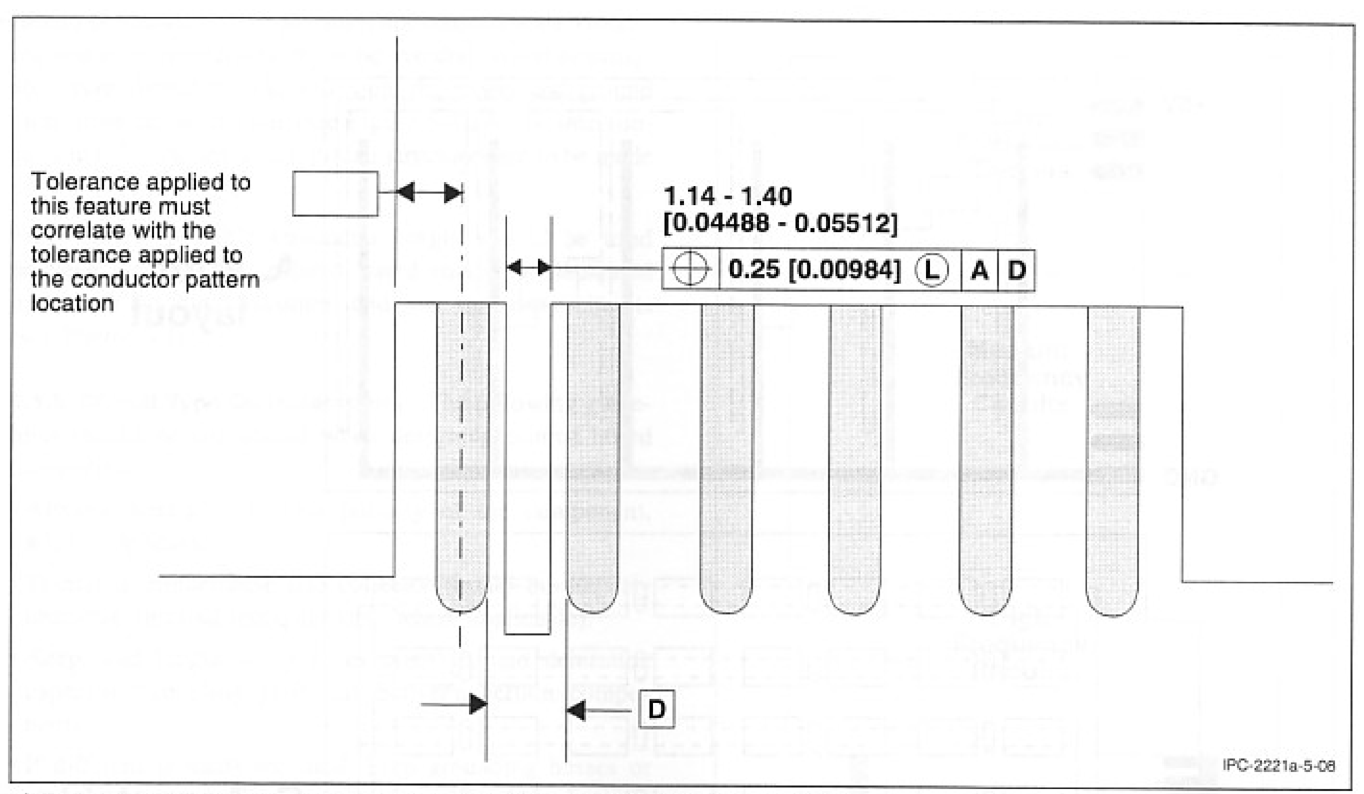


Figure 5-8 Example of Connector Key Slot Location and Tolerance, mm [in]

6 ELECTRICAL PROPERTIES

6.1 Electrical Considerations

6.1.1 Electrical Performance When printed-board assemblies are to be conformal coated, they **shall** be constructed, adequately masked, or otherwise protected in such a manner that application of the conformal coating does not degrade the electrical performance of the assembly. High speed circuit designs should consider the recommendations of IPC-D-317.

6.1.2 Power Distribution Considerations A predominately important factor that should be considered in the design of a printed board is power distribution. The grounding scheme can be used as a part of the distribution system. It provides not only a DC power return, but also an AC reference plane for high-speed signals to be referenced. The following items should be taken into consideration.

Maintain a lower radio-frequency (RF) impedance throughout the DC power distribution. An improperly designed ground can result in RF emissions. This results from radiated field gradients developed across the uneven board impedance and its inability of decoupling capacitors to efficiently reduce the board's EMI.

Decouple the power distribution at the printed board connector using adequate decoupling capacitance. Distribute adequate individual power/ground decoupling capacitors evenly throughout logic device board areas. Minimize the impedance and radiation loop of the coupling capacitor by keeping capacitor leads as short as possible, and locating them adjacent to the critical circuit.

A good technique for the distribution of power and grounds in a multilayer board is to use planes. When utilizing planes for power and ground distribution, it is recommended that the incoming power and ground signals terminate at the input decoupling network, prior to connecting to the respective internal planes. If external power busses are required, commercially available bussing schemes may be employed as defined in 8.2.13. When using power conductors, as shown in Figure 6-1, power traces should be run as close as possible to ground traces. Both power and ground traces **shall** be maintained as wide as possible. The power and ground planes virtually become one plane at high frequencies, and should, therefore, be kept next to each other.

Figure 6-1A shows a poor layout, giving high inductance and few adjacent signal return paths; this leads to crosstalk.

Figure 6-1B is a better layout and reduces power distribution, logic-return impedances, conductor crosstalk and board radiation.

The best layout is shown in Figure 6-1C, which has further EMI problem reductions.

In digital power distribution schemes, the grounding and power should be designed first, not last, as is typically done with some analog circuits. All interfacing, including power,

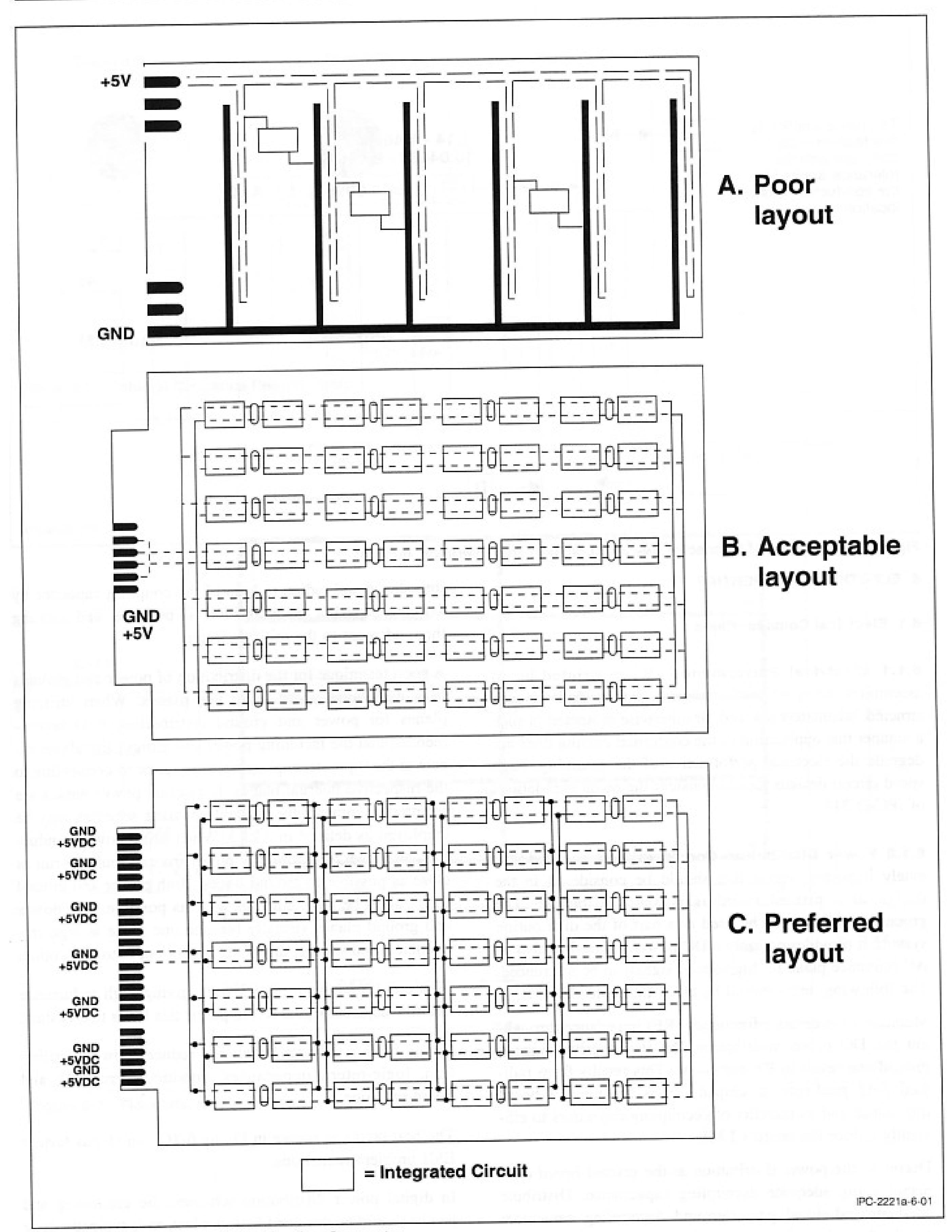


Figure 6-1 Voltage/Ground Distribution Concepts

should be routed to a single reference edge, or area. Opposing end interconnections are to be avoided. When unavoidable, care should be taken to route the power and ground away from active circuits (see Figure 6-2). At the interconnection reference edge, all ground structures are to be made as heavy as possible.

The shortest possible conductor length should be used between devices. The printed board should be separated into areas for high, medium, and low frequency circuits (see Figure 6-3).

6.1.3 Circuit Type Considerations The following guidelines should be considered when designing printed board assemblies:

- Always determine correct polarity of the component, where applicable.
- Transistor emitter/base and collector should be properly identified (ground transistor case where applicable).
- Keep lead length as short as possible, and determine capacitive coupling problems between certain components.
- If different grounds are used, keep grounding busses or planes as far away from each other as possible.
- As opposed to digital signals, analog design should have signal conductors considered first, and ground planes or ground conductor connections considered last.

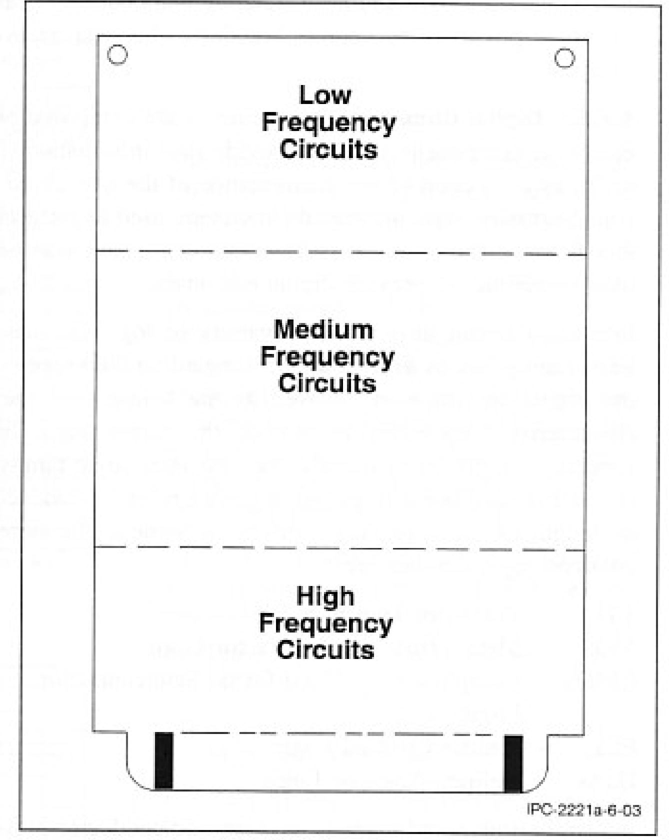


Figure 6-3 Circuit Distribution

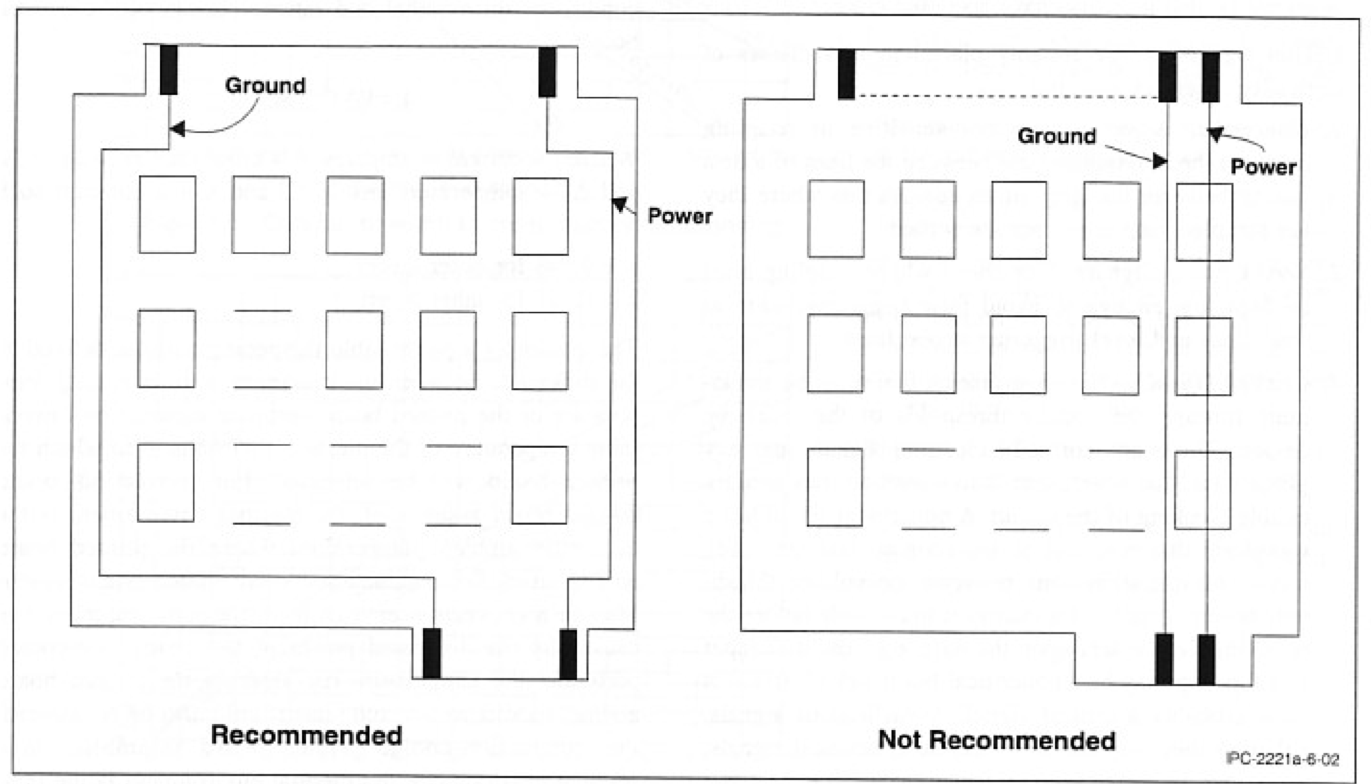


Figure 6-2 Single Reference Edge Routing

• Keep heat-sensitive and heat-radiating components as far apart as possible (incorporate heatsinks whenever necessary).

6.1.3.1 Digital Circuits Digital circuits are composed of electronic components that can provide state information (1 or 0), as a function of the performance of the overall circuit. Normally, logic integrated circuits are used to perform this function; however, discrete components may also be used sometimes to provide digital responses.

Integrated circuit devices use a variety of logic families. Each family has its own parameters regarding the speed of the digital transmission, as well as the temperature rise characteristics necessary to provide the performance. In general, a single board usually uses the same logic family in order to facilitate a single set of design rules for conductor length for signal driving restrictions. Some of the more common logic families are:

TTL – Transistor Transistor Logic
MOS – Metal Oxide Semiconductor Logic
CMOS – Complimentary Metal Oxide Semiconductor Logic
ECL – Emitter Coupled Logic
GaAs – Gallium Arsenide Logic

In certain high-speed applications, specific conductor routing rules may apply. A typical example is serial routing between signal source, loads and terminators. Rating branches (stubs) may also have specified criteria.

Digital signals can be roughly placed in four classes of criticality. These classes are:

1. *Noncritical Signals* – are not sensitive to coupling between them. Examples are between the lines of a data bus or between the lines of an address bus where they are sampled long after they are settled.
2. *Semi-Critical Signals* – are those where coupling must be kept low enough to avoid false triggering, such as reset lines and level triggering strobe lines.
3. *Critical Signals* – have waveforms that must be monotonic through the voltage thresholds of the receiving device. These are normally clocking signals and any glitch while the wave form is in transition may cause a double clocking of the circuit. A noncritical signal has a waveform that need not be monotonous and may even make multiple transitions between the voltage thresholds before it settles. Obviously it must settle before the receiving device acts upon the data, e.g., the data input to a flip-flop may be a noncritical but the clock signal is most probably a critical signal. Asynchronous signals, although they may (or may not) be noncritical signals, should not be mixed with critical signals since there is a real possibility of the asynchronous signals inducing noise on the critical signals during the clock transitions. Clock signals that do not have a common master frequency should also not be routed together for similar reasons.
4. *Super-Critical Signals* – are those in applications such as clocks or strobes for A/D and D/A converters, signals in Phase Locked Loops, etc. In these types of applications phase lock jitters and crosstalk, causing errors, noise and timing jitters, will show up in the application's output performance. It is only a question of the amount of disturbance within the required performance specification. This class of signal is essentially the same as an analog coupling situation. In other words, it is completely linear (the total noise is the sum of the individual noise elements; no averaging or canceling out can be assumed).

6.1.3.2 Analog Circuits Analog circuits are usually made from integrated circuits and discrete devices. Standard discrete components (resistors, capacitors, diodes, transistors, etc.), as well as power transformers, relays, coils and chokes, are usually the types of discrete devices used for analog circuits.

6.2 Conductive Material Requirements The minimum width and thickness of conductors on the finished board **shall** be determined primarily on the basis of the current-carrying capacity required, and the maximum permissible conductor temperature rise. The minimum conductor width and thickness **shall** be in accordance with Figure 6-4 for conductors on external and internal layers of the printed board.

$$I = k\Delta T^{0.44}A^{0.725}$$

Where I = current in amperes, A = cross section in sq. mils, and ΔT = temperature rise in °C and k is a constant such that:

k = 0.048 for outer layers
k = 0.024 for inner layers

The conductor's permissible temperature rise is defined as the difference between the maximum safe operating temperature of the printed board laminate material and maximum temperature of the thermal environment to which the printed board will be subjected. For convection-cooled printed board assemblies, the thermal environment is the maximum ambient temperature where the printed board will be used. For conduction-cooled printed board assemblies in a convection environment, the temperature rise is caused by the dissipated power of the conduction-cooled parts and the temperature rise through the printed board and/or heatsink to the cold plate should also be considered. For conduction-cooled printed board assemblies in a vacuum environment, the thermal environment is the temperature rise caused by the dissipated power of the parts and the temperature rise through the printed board and/or heatsink to the cold plate. In a vacuum environment, the

(For use in determining current carrying capacity and sizes of etched copper conductors for various temperature rises above ambient.)

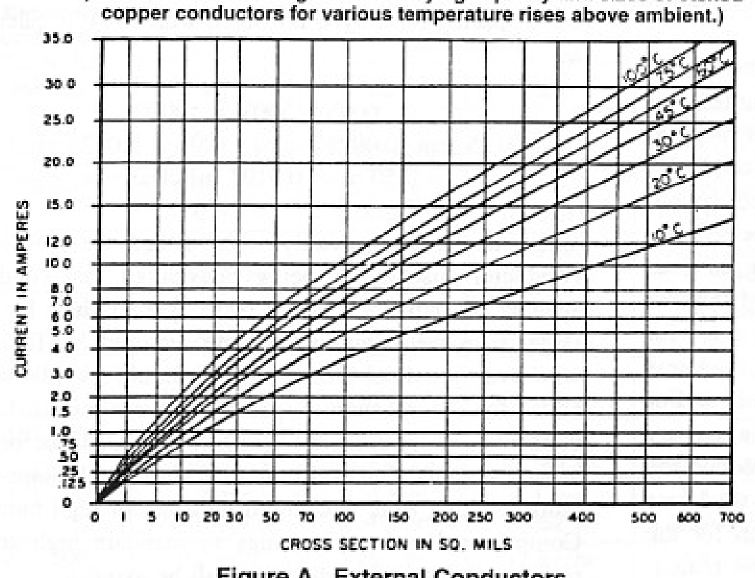


Figure A External Conductors

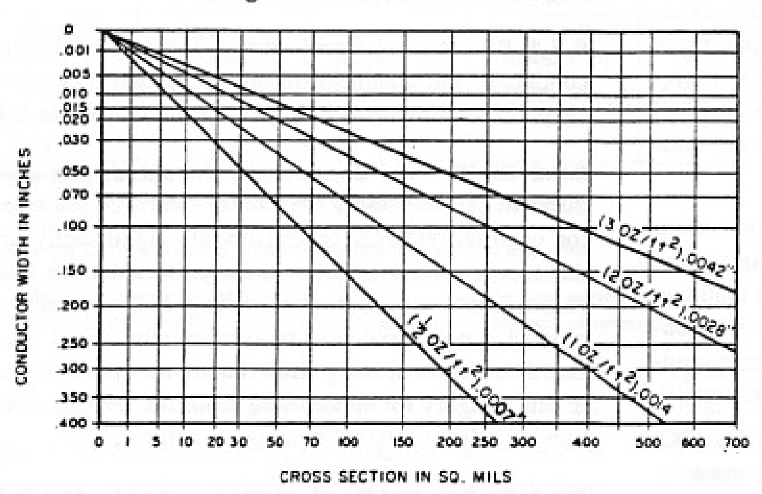


Figure B Conductor width to cross-section relationship

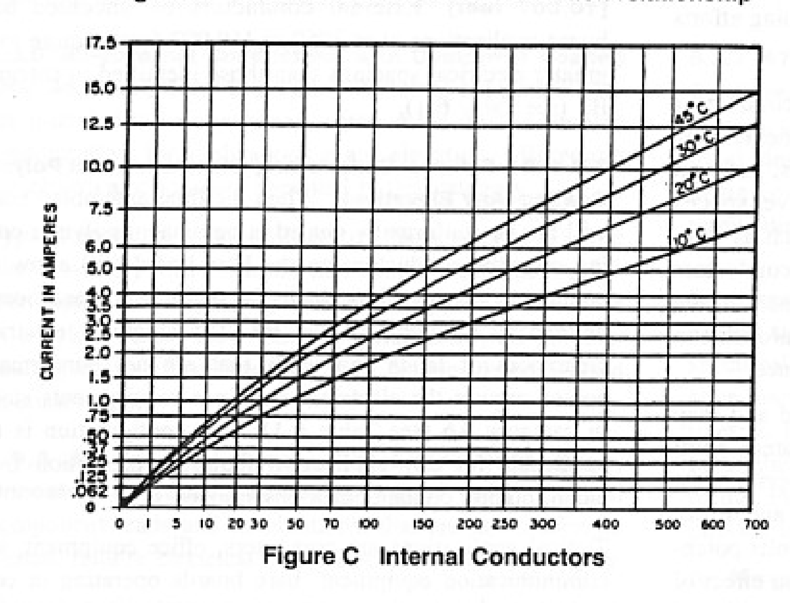


Figure C Internal Conductors

Notes:

1. The design chart has been prepared as an aid in estimating temperature rises (above ambient) vs. current for various cross-sectional areas of etched copper conductors. It is assumed that, for normal design, conditions prevail where the conductor surface area is relatively small compared to the adjacent free panel area. The curves as presented include a nominal 10 percent derating (on a current basis) to allow for normal variations in etching techniques, copper thickness, conductor width estimates, and cross-sectional area.
2. Additional derating of 15 percent (current-wise) is suggested under the following conditions:
   (a) For panel thickness of 0.8 mm [0.031 in] or less
   (b) For conductor thickness of 108 µm [4252 µin] or thicker.
3. For general use the permissible temperature rise is defined as the difference between the ambient temperature and the maximum sustained operating temperature of the assembly.
4. For single conductor applications the chart may be used directly for determining conductor widths, conductor thickness, cross-sectional area, and current-carrying capacity for various temperature rises.
5. For groups of similar parallel conductors, if closely spaced, the temperature rise may be found by using an equivalent cross-section and an equivalent current. The equivalent cross-section is equal to the sum of the cross-section of the parallel conductors, and the equivalent current is the sum of the currents in the conductors.
6. The effect of heating due to attachment of power dissipating parts is not included.
7. The conductor thicknesses in the design chart do not include conductor overplating with metals other than copper.

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Figure 6-4 Conductor Thickness and Width for Internal and External Layers

effects of radiation heat transfer between the parts, the printed board assembly and the cold plate should also be considered.

For internal layers, the conductor thickness is the copper foil thickness of the base laminate unless blind/buried vias are used in which case the copper foil thickness includes copper process plating. For external layers, the conductor thickness also includes the thickness of plated copper deposited during the plated-through hole process, but should not include the thickness of solder coating, tin-lead plating, or secondary platings. It should be noted that the foil thickness specified by the standard drawing noted for the preferred printed board materials are nominal thickness values which can generally vary by as much as ± 10%. For external layers, the total copper thickness will also vary due to processing prior to plating which may reduce the thickness of base copper. Furthermore, since the thickness of plated copper is controlled by the requirement for the thickness of copper required in the barrel of the plated-through hole, the associated amount of copper on the external layers may not be the same thickness as the plating in the barrels of the plated-through holes (see 10.1.1). Therefore, if conductor thickness is critical, a minimum finished board conductor thickness should be specified on the master drawing.

For ease of manufacture and durability in usage, these parameters should be optimized while maintaining the minimum recommended spacing requirements. To maintain finished conductor widths, as on the master drawing, conductor widths on the production master may require compensation for process allowances as defined in Section 10.

At the time of publication of the A revision to the IPC-2221, an update of the conductor current carrying capacity charts was underway. See Appendix B for a discussion and clarification of the existing charts as well as ongoing efforts to update them.

6.3 Electrical Clearance Spacing between conductors on individual layers should be maximized whenever possible. The minimum spacing between conductors, between conductive patterns, layer to layer conductive spaces (z=axis), and between conductive materials (such as conductive markings or mounting hardware) and conductors **shall** be in accordance with Table 6-1, and defined on the master drawing. See Section 10 for additional information on process allowances affecting electrical clearance.

When mixed voltages appear on the same board and they require separate electrical testing, the specific areas **shall** be identified on the master drawing or appropriate test specification. When employing high voltages and especially AC and pulsed voltages greater than 200 volts potential, the dielectric constant and capacitive division effect of the material must be considered in conjunction with the recommended spacing.

For voltages greater than 500V, the (per volt) table values must be added to the 500V values. For example, the electrical spacing for a Type B1 board with 600V is calculated as:

600V - 500V = 100V
0.25 mm [0.00984 in] + (100V x 0.0025 mm)
= 0.50 mm [0.0197 in] clearance

When, due to the criticality of the design, the use of other conductor spacings is being considered, the conductor spacing on individual layers (same plane) **shall** be made larger than the minimum spacing required by Table 6-1 whenever possible. Board layout should be planned to allow for the maximum spacing between external layer conductive areas associated with high impedance or high voltage circuits. This will minimize electrical leakage problems resulting from condensed moisture or high humidity. Complete reliance on coatings to maintain high surface resistance between conductors **shall** be avoided.

6.3.1 B1–Internal Conductors Internal conductor-to-conductor, and conductor-to-plated-through hole electrical clearance requirements at any elevation (see Table 6-1).

6.3.2 B2–External Conductors, Uncoated, Sea Level to 3050 m [10,007 feet] Electrical clearance requirements for uncoated external conductors are significantly greater than for conductors that will be protected from external contaminants with conformal coating. If the assembled end product is not intended to be conformally coated, the bare board conductor spacing **shall** require the spacing specified in this category for applications from sea level to an elevation of 3050 m [10,007 feet] (see Table 6-1).

6.3.3 B3–External Conductors, Uncoated, Over 3050 m [10,007 feet] External conductors on uncoated bare board applications over 3050 m [10,007 feet] require even greater electrical spacings than those identified in category B2 (see Table 6-1).

6.3.4 B4–External Conductors, with Permanent Polymer Coating (Any Elevation) When the final assembled board will not be conformally coated, a permanent polymer coating over the conductors on the bare board will allow for conductor spacings less than that of the uncoated boards defined by category B2 and B3. The assembly electrical clearances of lands and leads that are not conformally coated require the electrical clearance requirements stated in category A6 (see Table 6-1). This configuration is not applicable for any application requiring protection from harsh, humid, contaminated environments.

Typical applications are computers, office equipment, and communication equipment, bare boards operating in controlled environments in which the bare boards have a permanent polymer coating on both sides. After they are

Table 6-1 Electrical Conductor Spacing

Voltage Between Conductors (DC or AC Peaks)	Minimum Spacing						
	Bare Board				Assembly		
	B1	B2	B3	B4	A5	A6	A7
0-15	0.05 mm [0.00197 in]	0.1 mm [0.0039 in]	0.1 mm [0.0039 in]	0.05 mm [0.00197 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]
16-30	0.05 mm [0.00197 in]	0.1 mm [0.0039 in]	0.1 mm [0.0039 in]	0.05 mm [0.00197 in]	0.13 mm [0.00512 in]	0.25 mm [0.00984 in]	0.13 mm [0.00512 in]
31-50	0.1 mm [0.0039 in]	0.6 mm [0.024 in]	0.6 mm [0.024 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.4 mm [0.016 in]	0.13 mm [0.00512 in]
51-100	0.1 mm [0.0039 in]	0.6 mm [0.024 in]	1.5 mm [0.0591 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.5 mm [0.020 in]	0.13 mm [0.00512 in]
101-150	0.2 mm [0.0079 in]	0.6 mm [0.024 in]	3.2 mm [0.126 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
151-170	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	3.2 mm [0.126 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
171-250	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	6.4 mm [0.252 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
251-300	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	12.5 mm [0.4921 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.8 mm [0.031 in]
301-500	0.25 mm [0.00984 in]	2.5 mm [0.0984 in]	12.5 mm [0.4921 in]	0.8 mm [0.031 in]	0.8 mm [0.031 in]	1.5 mm [0.0591 in]	0.8 mm [0.031 in]
> 500 See para. 6.3 for calc.	0.0025 mm /volt	0.005 mm /volt	0.025 mm /volt	0.00305 mm /volt	0.00305 mm /volt	0.00305 mm /volt	0.00305 mm /volt

B1 - Internal Conductors
B2 - External Conductors, uncoated, sea level to 3050 m [10,007 feet]
B3 - External Conductors, uncoated, over 3050 m [10,007 feet]
B4 - External Conductors, with permanent polymer coating (any elevation)
A5 - External Conductors, with conformal coating over assembly (any elevation)
A6 - External Component lead/termination, uncoated, sea level to 3050 m [10,007 feet]
A7 - External Component lead termination, with conformal coating (any elevation)

assembled and soldered the boards are not conformal coated, leaving the solder joint and soldered land uncoated.

Note: All conductors, except for soldering lands, must be completely coated in order to ensure the electrical clearance requirements in this category for coated conductors.

6.3.5 A5–External Conductors, with Conformal Coating Over Assembly (Any Elevation) External conductors that are intended to be conformal coated in the final assembled configuration, for applications at any elevation, will require the electrical clearances specified in this category.

Typical applications are military products where the entire final assembly will be conformal coated. Permanent polymer coatings are not normally used, except for possible use as a solder resist. However, the compatibility of polymer coating and conformal coating must be considered, if used in combination.

6.3.6 A6–External Component Lead/Termination, Uncoated, Sea Level to 3050 m [10,007 feet] External component leads and terminations, that are not conformal coated, require electrical clearances stated in this category.

Typical applications are as previously stated in category B4. The B4/A6 combination is most commonly used in commercial, nonharsh environment applications in order to obtain the benefit of high conductor density protected with permanent polymer coating (also solder resist), or where the accessibility to components for rework and repair is not required.

6.3.7 A7–External Component Lead/Termination, with Conformal Coating (Any Elevation) As in exposed conductors versus coated conductors on bare board, the electrical clearances used on coated component leads and terminations are less than for uncoated leads and terminations.

6.4 Impedance Controls Multilayer printed boards are ideally suited for providing interconnection wiring that is specifically designed to provide desired levels of impedance and capacitance control. Techniques commonly referred to as "stripline," or "embedded microstrip," are particularly suited for impedance and capacitance requirements. Figure 6-5 shows four of the basic types of transmission line constructions. These are:

A. *Microstrip* – A rectangular trace or conductor placed at the interface between two dissimilar dielectrics (usually air and usually FR-4) whose main current return path

(usually a solid copper plane) is on the opposite side of the high-εr material. Three sides of the conductor contact the low-εr materials ($\varepsilon r = 1$), and one side of the conductor contacts the high-εr material ($\varepsilon r > 1$).

B. *Embedded Microstrip* – Similar to Microstrip except that the conductor is completely embedded in the higher-εr materials.

C. *Symmetric Stripline* – A rectangular trace or conductor surrounded completely by a homogeneous dielectric medium and located symmetrically between two reference planes.

D. *Dual (Asymmetric) Stripline* – Similar to Stripline except that one or more conductor layers are asymmetrically located between the two reference planes.

The design of such multilayer printed boards should take into consideration the guidelines of IPC-D-317 and IPC-2141.

6.4.1 Microstrip Flat conductors are the geometry normally found on a printed board as manufactured by the copper plating and etching processes (see Figure 6-5A). The capacitance is influenced most strongly by the region between the signal line and adjacent ground (or power) planes. Inductance is a function of the "loop" formed by the frequency of operation (i.e., skin effect) and the distance to the reference plane for microstrips and striplines, and the length of the conductor.

The following equations give the impedance (Z_0) propagation delay (T_{pd}), and intrinsic line capacitance (C_0) for microstrip circuitry.

$$Z_0 = \frac{87}{\sqrt{\varepsilon r + 1.41}} \ln\left[\frac{5.98h}{0.8w + t}\right] \quad \text{in ohms}$$

$$T_{pd} = \frac{\sqrt{\varepsilon r}}{c} \quad \text{in psec/inch}$$

$$C_0 = \frac{T_{pd}}{Z_0} \quad \text{in pF/inch}$$

$$\text{For } \frac{w}{h} < 1$$

where:

c = Speed of light in vacuum (3.0×10^8 m/s)
h = Dielectric thickness, inches
w = Line width, inches
t = Line thickness, inches
εr = Relative permittivity (dielectric constant) of substrate (see Table 6-2)

The radiated electromagnetic interference (EMI) signal from the lines will be a function of the line impedance, the length of the signal line and the incident waveform characteristics. This may be an important consideration in some high speed circuitry. In addition, crosstalk between adjacent circuits will depend directly upon circuit spacing, the distance to the reference planes, length of parallelism between conductors, and signal rise time (see IPC-D-317).

6.4.2 Embedded Microstrip Embedded microstrip has the same conductor geometry as the uncoated microstrip discussed above. However, the effective dielectric constant is different because the conductor is fully enclosed by the dielectric material (see Figure 6-5B). The equations for embedded microstrip lines are the same as in the section on [uncoated] microstrip, with a modified effective dielectric constant. If the dielectric thickness above the conductor is 0.025 mm [0.0009843 in] or more, then the effective dielectric constant can be determined using the criteria in IPC-D-317. For very thin dielectric coatings (less than 0.025 mm [0.0009843 in]), the effective dielectric constant will be between that for air and the bulk dielectric constant (see Table 6-2).

6.4.3 Stripline Properties A stripline is a thin, narrow conductor embedded between two AC ground planes (Figure 6-5C). Since all electric and magnetic field lines are contained between the planes, the stripline configuration has the advantage that EMI will be suppressed except for lines near the edges of the printed board. Crosstalk between circuits will also be reduced (compared to the microstrip case) because of the closer electrical coupling of each circuit to ground. Because of the presence of ground planes on both sides of a stripline circuit, the capacitance of the line is increased and the impedance is decreased from the microstrip case.

Stripline impedance (Z_0) and intrinsic line capacitance (C_0) parameters are presented below for flat-conductor geometries. The equations assume that the circuit layer is placed midway between the planes.

$$Z_0 = \frac{60 \ln\left[\frac{1.9\,(2H + T)}{(0.8W + T)}\right]}{\sqrt{\varepsilon r}} \quad \text{in ohms}$$

$$C_0 = \frac{1.41\,(\varepsilon r)}{\ln\left[\frac{3.81H}{(0.8W + T)}\right]} \quad \text{in pF/in}$$

$$\text{For } \frac{W}{H} < 2$$

where:

H = Distance between line and one ground plane
T = Line thickness inches
W = Line width inches
εr = Relative permittivity of substrate
pF = Picofarads

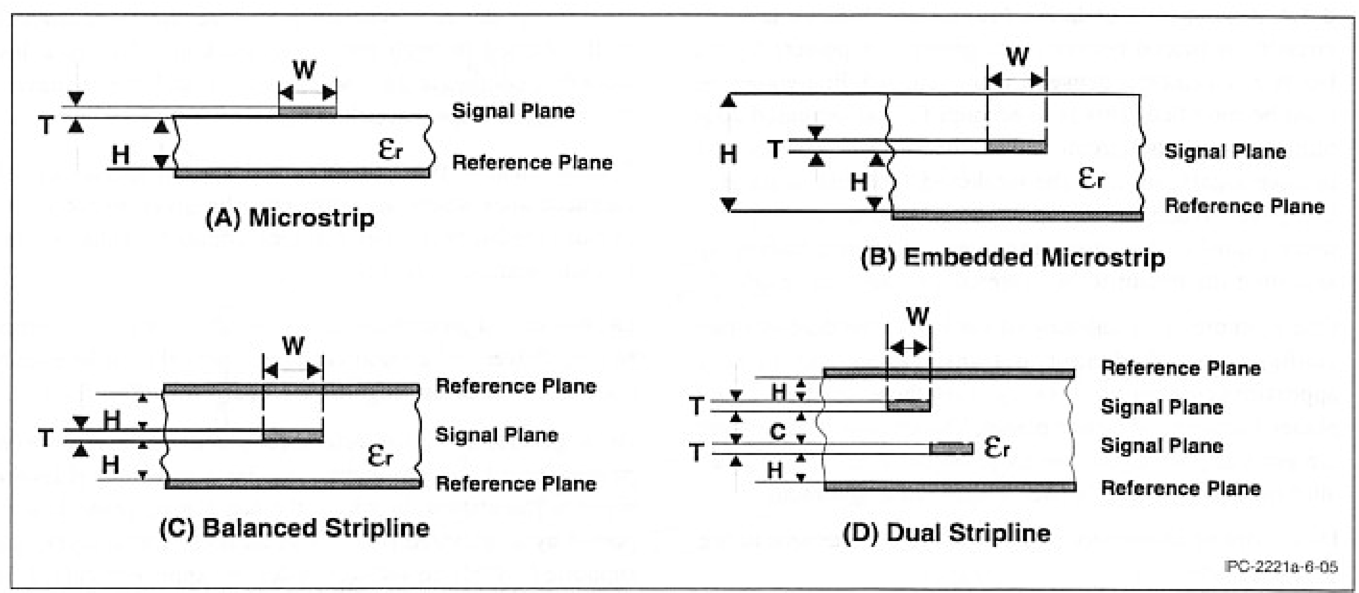


Figure 6-5 Transmission Line Printed Board Construction

Table 6-2 Typical Relative Bulk Dielectric Constant of Board Material

DESIGNATOR					RESIN REF. CODE	Material Reinforcement/Resin	Dielectric Constant
	IPC SPECIFICATION			MILITARY [2]			
NEMA [1]	4202	4101	4103	S-13949			Er value [3]
G-10		/20		/3	GEN	Woven E Glass/Epoxy	4.6-5.4
G-11		/22		/2	GB	Woven E Glass/Epoxy	4.5-5.4
FR-4[4]		/24		/4	GF GFN GFK	Woven E Glass/Epoxy	4.2-4.9
FR-5		/23		/5	GH	Woven E Glass/Epoxy	4.2-4.9
GPY		/42		/10	GI GIJ	Woven E Glass/Polyimide	4.0-4.7
		/50		/15	AF	Woven Aramid/Modified Epoxy	3.8-4.5
		/55		/22	BF	Nonwoven Aramid/Epoxy	3.8-4.5
		/53		/31	BI	Nonwoven Aramid/Polyimide	3.6-4.4
		/60		/19	QIL	Woven Quartz/Polyimide	3.0-3.8
		/30		/24	GM GFT	Woven E Glass/Triazine/BT	4.0-4.7
		/71		/29	GC	Woven E Glass/Cyanate Ester	4.0-4.7
			4103/03	/6	GP	Nonwoven Glass/PTFE	2.15-2.35
			4103/04	/7	GR	Nonwoven Glass/PTFE	2.15-2.35
			4103/01	/8	GT	Woven Glass/PTFE	2.45-2.65
			4103/02	/9	GX	Woven Glass/PTFE	2.4-2.6
			4103/05	/14	GY	Woven Glass/PTFE	2.15-2.35
	/1 [5]					Nonsupported Polyimide	3.2-3.6

Note: Dielectric values will vary approximately within the range given, depending on the reinforcement/resin ratio. Generally thin laminates tend toward the lower values.

1. National Electrical Manufacturers Association. Several NEMA grades, such as the paper/paper composite based products XPC, FR-1, FR-2, CEM, etc. have been omitted from this table. See IPC-4101 for complete cross-reference and properties of these grades.
2. MIL-S-13949 is canceled and listed for reference only.
3. Permittivity @ 1 MHZ maximum. (Laminate or prepreg as laminated)
4. Multiple slash sheet designations exist within IPC-4101 for the FR-4 classification. See IPC-4101 /21, /25, /26, /82 for specific differences of resin formulations and T_g values.
5. Polyimide flexible film is listed for comparison to reinforced materials; additional properties of flexible films with coatings and cladding can be found in IPC-4203 and 4204 respectfully. See also IPC-2223 for applications.

6.4.4 Asymmetric Stripline Properties When a layer of circuitry is placed between two ground (or power) layers, but is not centered between them, the stripline equations must be modified. This is to account for the increased coupling between the circuit and the nearest plane, since this is more significant than the weakened coupling to the distant plane. When the circuit is placed approximately in the middle third of the interplane region, the error caused by assuming the circuit to be centered will be quite small.

One example of an unbalanced stackup is the dual stripline configuration. A dual-strip transmission line closely approximates a stripline except that there are two signal planes between the power planes. The circuits on one layer are generally orthogonal to those on the other to keep parallelism and crosstalk between layers to a minimum.

Dual stripline impedance (Z_0) and intrinsic line capacitance (C_0) parameters are:

$$Z_0 = \frac{80 \ln\left[\frac{1.9\,(2H+T)}{(0.8W+T}\right] \cdot \left[1 - \frac{H}{4\,(H+C+T)}\right]}{\sqrt{\varepsilon r}} \quad \text{in ohms}$$

$$C_0 = \frac{2.82\,(\varepsilon r)}{\left[\frac{2H-T}{(0.268W+0.335T)}\right]} \quad \text{in pF/in}$$

where:

H = Height above power plane
C = Signal plane separation
T = Line thickness, inches
W = Line width, inches
pF = Picofarads

This stackup is shown in Figure 6-5D. As with stripline, EMI will be completely shielded except for signal lines near the edges of the printed board.

The above equations can be adapted to determine Z_0 or C_0 for asymmetric stripline circuits that are not dual stripline. Plane sequences for a four-layer board should be as described in Figure 6-5D. For boards with more than four layers, the sequence should be arranged so that the signal layers are symmetrical about the ground or voltage plane. This may be accomplished several ways provided that any adjacent signal layers, not separated by a ground or voltage plane should have their key axes running perpendicular to each other. For a 6-layer board, the sequence might be:

A		B
Signal #1		Signal #1
Plane #1		Signal #2
Signal #2	or	Plane #1
Signal #3		Plane #2
Plane #2		Signal #3
Signal #4		Signal #4

"A" is the desired configuration since the impedance is well matched through the entire stack-up. "B" is a less desirable configuration since signals 1 and 4 will have a much higher impedance than signals 2 and 3.

Special attention is required in the design of specific circuit characteristics where attention must be given to total conductor lengths, both short and long conductor runs, as well as total interconnection routing.

DC power and ground planes also function as AC reference planes. Power and ground connector pins should be evenly distributed along the edge of the board for AC reference.

As a general rule, the reference planes of a multilayer printed board design should not be segmented. Limited plane segmentation, in which the segmented plane is supported by an elevated plane to an adjacent signal layer, and supported by plated-through holes on approximately 2.54 mm [0.1 in] centers on both sides, may be used to "bury" a special high frequency signal within the planes to create a "coaxial type" line within the board. Spacing of the holes is dependent on frequency of the signal.

6.4.5 Capacitance Considerations Figures 6-6 and 6-7 show the intrinsic line capacitance/per unit length, of copper, for microstrip and stripline, respectively. These charts provide capacitance in pF/ft for 1 oz. copper conductors with various dielectric thicknesses to the ground or power reference plane. Figure 6-7 for stripline is based upon symmetry with the conductor centered between the reference ground and power planes.

The capacitance associated with single crossover (see Figure 6-8) is very small and is typically a fraction of a picofarad. As the number of crossovers per unit length increases, the intrinsic capacitance of the transmission line also increases. The crossover lumped capacitance adds to the intrinsic line capacitance. Crossover capacitance (C_c) may be approximated by:

$$C_c = X\varepsilon_r(l + 0.8h)\,\frac{(W + 0.8h)}{h} \quad \text{in pF}$$

provided that $l \geq 0.5h$

$W \geq 0.5h$

where:

X = 0.0089 if h, l and W are in mm, 0.225 if h, l and W are in inches
εr = relative permittivity
h = dielectric thickness between crossovers
l = length
W = Width

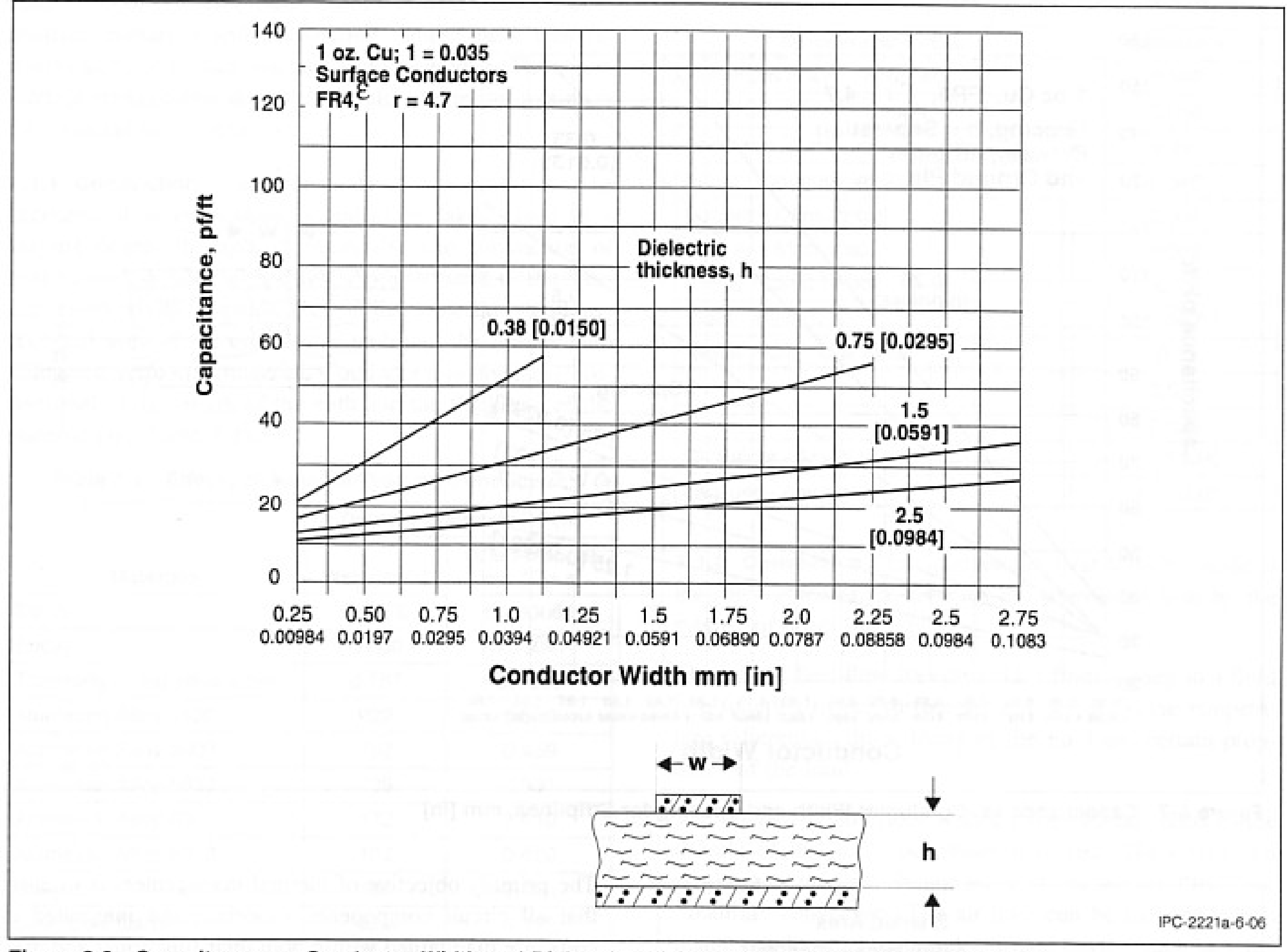


Figure 6-6 Capacitance vs. Conductor Width and Dielectric Thickness for Microstrip Lines, mm [in]

6.4.6 Inductance Considerations Inductance is the property of a conductor that allows it to store energy in a magnetic field induced by a current flowing through that conductor. When this current has high frequency components, the self-inductance of the leads and traces become significant, leading to transient or switching noise. These transients are related to the inductance of a power/ground loop and the circuit must be designed to reduce this inductance as much as possible.

A common technique to reduce this switching noise is the use of decoupling capacitors that serve to provide the current from a point closer to the IC gate than the power supply. Even when these capacitors are designed into the circuit, the positioning of the capacitor is important. If the capacitor leads are too long, the self inductance becomes too high leading to switching noise. Decoupling on the boards is normally achieved with discrete capacitors that can be closely positioned to the IC. In higher I/O packages, a trend has begun which places the decoupling capacitor inside of the package. This has the double advantage of not using real estate for the capacitor location and reducing the size of the capacitor interconnections.

Another consideration is the use of smaller diameter via holes and their associated pad sizes. A change from 0.5 mm [0.020 in] vias to 0.3 mm [0.012 in] vias will reduce parasitic inductance in the circuit. Smaller diameter vias will improve it even more.

Closely spaced adjacent power and ground planes are also being utilized to provide high frequency decoupling capacitance. This also decreases the real estate required for decoupling capacitors.

1 oz Cu, FR4, Ɛr = 4.7
Spacing, h = Separation Between stripline and Ground Plane
Capacitance pF/ft
0.25 [0.00984]
0.33 [0.0130]
0.5 [0.020]
Spacing
0.75 [0.0295]
1.00 [0.03937]
1.25 [0.04921]
Conductor Width
w
h
IPC-2221a-6-07

Figure 6-7 Capacitance vs. Conductor Width and Spacing for Striplines, mm [in]

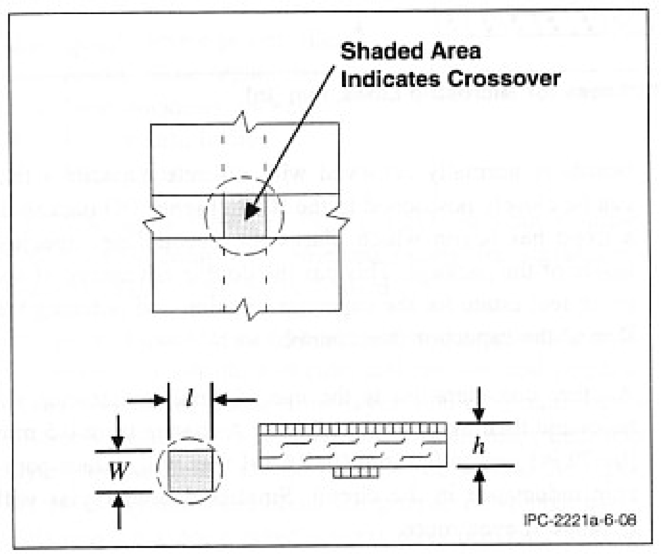


Figure 6-8 Single Conductor Crossover

7 THERMAL MANAGEMENT

This section is intended as an outline for temperature control and heat dissipation. This material, coupled with appropriate thermal analysis (see IPC-D-330), can result in greatly reduced thermal stresses and improved reliability of the components, solder attachment and the printed wiring board.

The primary objective of thermal management is to ensure that all circuit components, especially the integrated circuits, are maintained within both their functional and maximum allowable limits. The functional temperature limits provide the ambient temperature range of the component package (case), within which the electronic circuits can be allowed to properly perform.

The cooling technique to be used in the printed board assembly application must be known in order to ensure the proper printed board assembly design. For commercial applications, direct-air cooling (i.e., where cooling air contacts the printed board assembly) may be used.

For rugged and hostile environment usage, indirect cooling must be used to cool the printed board assembly. In this application, the assembly is mounted to the structure, that is air or liquid cooled, and the components are cooled by conduction to a heat-exchange surface. These designs must use appropriate metal heatsinks on the printed board assembly. Appropriate component mounting and bonding may be required. To ensure adequate design, thermal dissipation maps must be provided to aid analysis and thermal design of the printed board assembly.

7.1 Cooling Mechanisms The dissipation of the heat generated within electronic equipment results from the

interaction of the three basic modes of heat transfer: conduction, radiation and convection. These heat transfer modes can, and often do, act simultaneously. Thus, any thermal management approach should attempt to maximize their natural interaction.

7.1.1 Conduction The first mode of heat transfer to be encountered is conduction. Conduction takes place to a varying degree through all materials. The conduction of heat through a material is directly proportional to the thermal conductivity constant (K) of the material, the cross sectional area of the conductive path and the temperature difference across the material. Conduction is inversely proportional to the length of the path and the thickness of the material (see Table 7-1).

Table 7-1 Effects of Material Type on Conduction

Materials	Thermal Conductivity (K)	
	Watts/m °C	Gram-calorie/ cm °C • s
Still Air	0.0276	0.000066
Epoxy	0.200	0.00047
Thermally Conductive Epoxy	0.787	0.0019
Aluminum Alloy 1100	222	0.530
Aluminum Alloy 3003	192	0.459
Aluminum Alloy 5052	139	0.331
Aluminum Alloy 6061	172	0.410
Aluminum Alloy 6063	192	0.459
Copper	194	0.464
Steel Low Carbon	46.9	0.112

7.1.2 Radiation Thermal radiation is the transfer of heat by electromagnetic radiation, primarily in the infrared (IR) wavelengths. It is the only means of heat transfer between bodies that are separated by a vacuum, as in space environments.

Heat transfer by radiation is a function of the surface of the "hot" body with respect to its emissivity, its effective surface area and the differential to the fourth power of the absolute temperatures involved.

The emissivity is a derating factor for surfaces that are not "black bodies." It is defined as the ratio of emissive power of a given body to that of a black body, for which emissivity is unity (1.0). The optical color of a body has little to do with it being a "thermal black body." The emissivity of anodized aluminum is the same if it is black, red or blue. However, surface finish is important. A matte or dull surface will be more radiant than a bright or glossy surface (see Table 7-2).

Devices, components, etc. close to one another will absorb each other's radiant energy. If radiation is to be the principal means of heat transfer, "hot" spots must be kept clear of each other.

Table 7-2 Emissivity Ratings for Certain Materials

Material and Finish	Emissivity
Aluminum Sheet - Polished	0.040
Aluminum Sheet - Rough	0.055
Anodized Aluminum - any color	0.80
Brass - Commercial	0.040
Copper - Commercial	0.030
Copper - Machined	0.072
Steel - Rolled Sheet	0.55
Steel - Oxided	0.667
Nickel Plate - Dull Finish	0.11
Silver	0.022
Tin	0.043
Oil Paints - Any Color	0.92-0.96
Lacquer - Any Color	0.80-0.95

7.1.3 Convection The convection heat transfer mode is the most complex. It involves the transfer of heat by the mixing of fluids, usually air.

The rate of heat flow by convection from a body to a fluid is a function of the surface area of the body, the temperature differential, the velocity of the fluid and certain properties of the fluid.

The contact of any fluid with a hotter surface reduces the density of the fluid and causes it to rise. The circulation resulting from this phenomenon is known as "free" or "natural" convection. The air flow can be induced in this manner or by some external artificial device, such as a fan or blower. Heat transfer by forced convection can be as much as ten times more effective than natural convection.

7.1.4 Altitude Effects Convection and radiation are the principle means by which heat is transferred to the ambient air. At sea level, approximately 70% of the heat dissipated from electronic equipment might be through convection and 30% by radiation. As air becomes less dense, convective effects decrease. At 5200 m [17060.37 ft], the heat dissipated by convection may be less than half that of radiation. This needs to be considered when designing for airborne applications.

7.2 Heat Dissipation Considerations Design of multilayer boards to remove heat from a high thermal radiating printed board assembly should consider the use of:

- Heatsinking external planes (usually copper or aluminum).
- Heatsinking internal planes.
- Special heatsink fixtures.
- Connection to frame techniques.
- Liquid coolants and heatsink formation.

• Heat pipes.

• Heatsinking constraining substrates.

7.2.1 Individual Component Heat Dissipation Heatsinking of individual components can use a variety of different techniques. Section 8.1.10 of this standard provides information on some of the heatsinking devices that come with individual components requiring specific heat dissipation. In addition, consideration should be given to:

• Heatsink mounting (hardware or soldering).

• Thermal transfer adhesives, paste, or other materials.

• Solder temperature requirements.

• Cleaning requirements under heatsinks.

7.2.2 Thermal Management Considerations for Board Heatsinks The following factors must be addressed while the printed board components are being placed:

1. Method of heatsink mounting (e.g., adhesive bond, rivet, screw, etc.) to printed board.
2. Thickness of heatsink and printed board assembly to allow adequate component lead protrusion.
3. Automatic component insertion clearances (see Figure 7-1).
4. Heatsink material and material properties.
5. Heatsink finish (e.g., anodize, chemical film, etc.).
6. Component mounting methods (e.g., spacers, screw, bonding, etc.).
7. Heat transfer path and rate of heat transfer.
8. Producibility (e.g., method of assembly, method of cleaning, etc.).
9. Dielectric material required between the heatsink and any circuitry that may be designed on the heatsink mounting surface of the printed board.
10. Edge clearance to any exposed circuitry (i.e., component pads and circuit runs). Tooling hole location and size.
11. Heatsink shape as it relates to the structure of heatsink/ printed board assembly.
12. The heatsink should fully support the component. Do not allow the component the opportunity to tip during assembly or soldering.

Heatsinks **shall** be designed to avoid the occurrence of moisture traps and to allow access for post-soldering cleaning. This can be accomplished by providing accessible slots in the heatsink instead of round clearance holes under TO-204-AA, TO-213-AA, and similar packages with leads which extend through the heatsink and are soldered into the printed board.

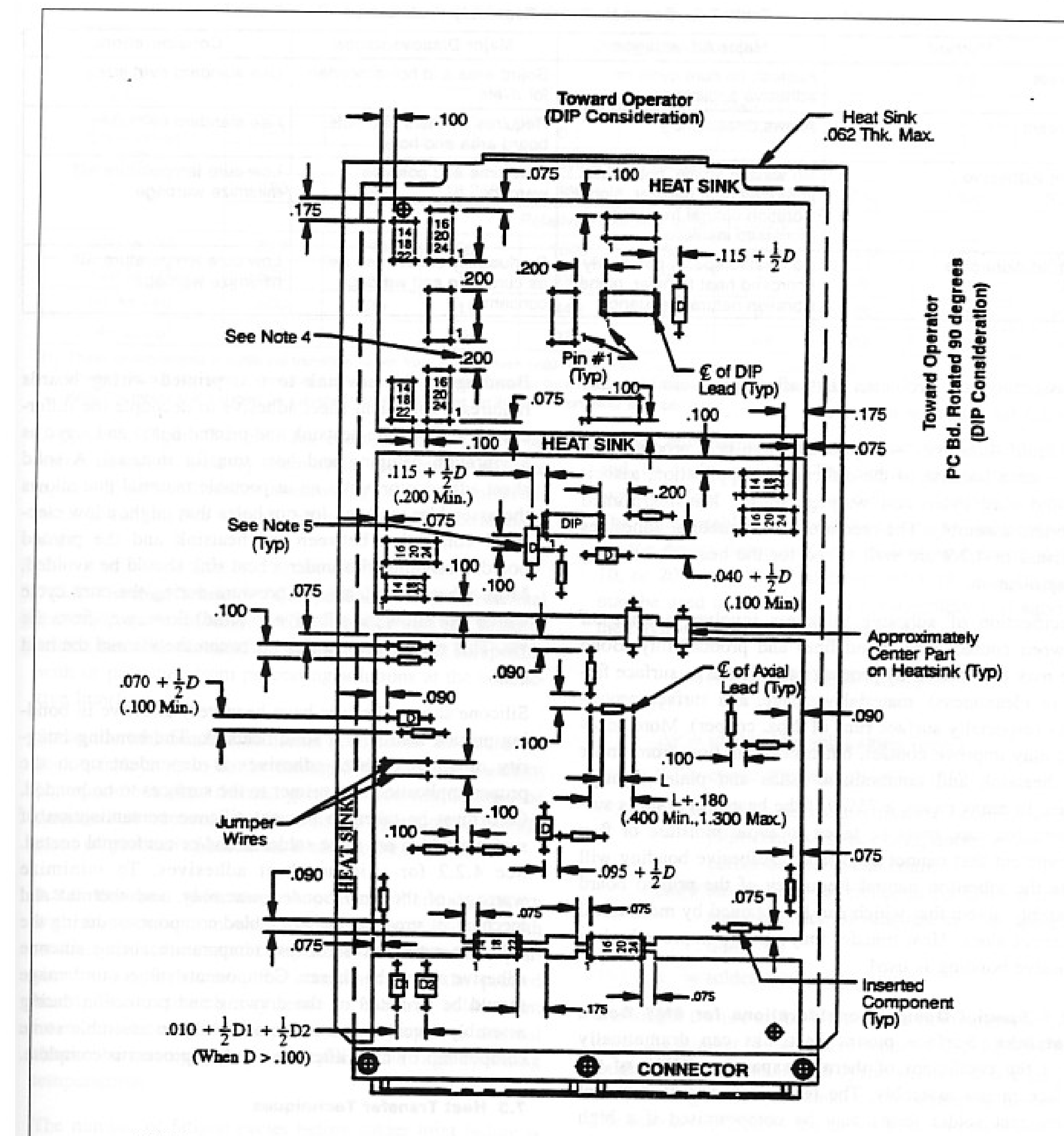
Through hole printed board assembly heatsinks generally are of a ladder configuration when standard component package types (i.e., DIPs and axial-leaded components) can be used. The ladder heatsink type is preferred due to its relative simplicity in design and fabrication. Figure 7-1 provides standard clearances between heatsink and components that are necessary to facilitate automatic component insertion.

Certain printed board assemblies (e.g., power supplies and other analog designs in particular) utilize many different component types. The circuit function for these analog circuits may be very dependent upon component placement. For analog designs, heatsinks sometimes cannot be designed in a ladder type configuration, however they should be designed with producibility in mind. Minimizing the number of unique cutout shapes required, and the number of areas where the heatsink thickness must change (requiring milling or lamination) will enhance heatsink producibility. When machined heatsinks are used efforts should be made to utilize as large a radius as possible in corners to enhance producibility (e.g., a 3.0 mm [0.118 in] radius can cost substantially more to fabricate than a 6.0 mm [0.236 in] radius). In all cases, analog heatsink designs that can't use ladders should be designed in parallel with the printed board (as opposed to after completion of artwork) and should be reviewed for producibility in both the metal fabrication and printed board assembly areas. Plated-through hole relief in the heat sink should be 2.5 mm [0.0984 in] larger than the hole, which includes electrical clearance and misregistration tolerance.

7.2.3 Assembly of Heatsinks to Boards Assembly of heatsinks to printed wiring boards may be accomplished as listed below (in order of manufacturing preference). If the board and the heatsink are purchased as an assembly, the manufacturer may have other preferences. Table 7-3 shows the preferences.

Details of these assembly methods are as follows:

1. *Mechanical Fasteners* – Riveting is the preferred fastening method, but care must be taken in rivet selection (solid or tubular), and rivet installation, to obviate laminate damage. Screws should be used if the unit is expected to be disassembled. Closer contact may be necessary to resist vibration or improve heat transfer. Use of adhesives along with mechanical fasteners can promote warpage but may help in a vibration environment. Dry film epoxy adhesives are preferred over liquids as the bond line thickness and squeeze-out is easy to control. Bonding temperatures should be as low as possible to minimize warpage.
2. *Film Type Adhesives* – Sheet adhesive is die or mechanically cut to fit the outline of the heatsink. The associated cure cycles and warpage of the heatsink/printed board



Notes:

1. Minimum dimensions are based on .032 maximum diameter copper leads. Larger leads and other lead materials to be considered on an individual basis.
2. Minimum dimensions shown provide for tool clearances, component body diameter must also be considered.
3. DIPs will be inserted prior to axial lead components.
4. When DIPs are inserted end to end, distances greater than .200 must be in increments of .100 (i.e., .200, .300, .400).
5. "D" represents maximum body diameter of indicated component.

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Figure 7-1 Component Clearance Requirements for Automatic Component Insertion on Through-Hole Technology Printed Board Assemblies [in]

Table 7-3 Board Heatsink Assembly Preferences

Method	Major Advantages	Major Disadvantages	Considerations
Rivets	Fastest, no cure cycle or adhesive application	Board area and holes needed for rivets	Use standard rivet sizes
Screws	Allows disassembly	Requires washers and nuts, board area and holes	Use standard hardware
Film Adhesive	No wasted space, potentially improved heat transfer, higher vibration natural frequency. Increased insulation	Cure time and possible warpage	Low cure temperature will minimize warpage
Liquid Adhesive	No wasted space, potentially improved heat transfer, higher vibration natural frequency	Producibility concern as well as cure time and warpage concern	Low cure temperature will minimize warpage

assembly are problems that affect producibility. See 4.2.3 for film type adhesives.

3. *Liquid Adhesives* – Liquid adhesive is a producibility concern because of the difficulty in application, associated cure cycle and warpage of the heatsink/printed board assembly. The recommended structural adhesives listed in 4.2.2 are well suited for the heatsink bonding application.

Specification of adhesive thickness involves a trade-off between contact area (bond line) and producibility. Bond line may be reduced by process variables (e.g., surface finish or cleanliness), material warpage, and surface protrusions (especially surface runs of 2 oz. copper). More adhesive may improve contact, but excess can flow from under the heatsink and contaminate lands and plated-through holes. In many cases, a 75% (of the heatsink) bond is sufficient, but care must be taken to avoid moisture or flux entrapment that cannot be cleaned. Adhesive bonding will raise the vibration natural frequency of the printed board assembly above that which can be obtained by mechanical fasteners alone. Heat transfer may also be improved when adhesive bonding is used.

7.2.4 Special Design Considerations for SMT Board Heatsinks Surface mount heatsinks can dramatically affect the coefficient of thermal expansion (CTE) of the surface mount assembly. The reliability of surface mount component solder joints may be compromised if a high CTE material is used, but depends upon the service environment of the surface mount assembly. Laboratory environments which do not subject the surface mount assembly to significant temperature changes may allow heatsink materials such as 1100 series aluminum to be used. Most environments require the use of low CTE heatsink materials to provide long solder joint life.

Heatsinks used in surface mount applications are either built within the printed board (typically copper-Invar-copper layers laminated in the printed board) or are a solid plate that has a surface mount printed board bonded to one or both sides.

Bonding of the heatsink to two printed wiring boards requires a compliant sheet adhesive to decouple the difference in CTE of the heatsink and printed board and serve as a vibration damping and heat transfer material. A solid sheet adhesive provides an inspectable material that allows the assembler to check for pin holes that might allow electrical connection between the heatsink and the printed board. Designing vias under a heat sink should be avoided. Most adhesive systems use pressure during the cure cycle which will allow the adhesive to (cold) flow away from the via. This can generate a short between the via and the heat sink.

Silicone sheet adhesives have been very effective in bonding printed boards to a solid heatsink. The bonding integrity of silicone sheet adhesives is dependent upon the proper application of a primer to the surfaces to be bonded. Care must be taken to prevent silicone contamination of surfaces which are to be soldered and/or conformal coated. See 4.2.2 for silicone sheet adhesives. To minimize warpage of the final bonded assembly, and thermal and mechanical stress on the assembled components during the adhesive cure process, a low temperature curing silicone adhesive should be chosen. Components subject to damage should be so noted on the drawing and protection during assembly required. It may be necessary to assemble some components by hand after the bonding process is complete.

7.3 Heat Transfer Techniques

7.3.1 Coefficient of Thermal Expansion (CTE) Characteristics For applications with surface mount components, the CTE of the interconnecting structure becomes an important consideration. Table 7-4 establishes calculated reliability figures of merit related to the differences in the X and Y expansion characteristics of the component and the substrates, the distance from the solder joint to the neutral point (zero strain point), and the solder joint height. This factor is related to the total strain per cycle of the solder joint. It is important to minimize the relative differences in the CTE of the component and printed board assembly. Typical ceramic substrates have a CTE from 5 to

Table 7-4 Comparative Reliability Matrix Component Lead/Termination Attachment

Cyclic Services Environment [°C]	Design Life [Years]								
	5			10			20		
	Cyclic Frequency [Cycles/Day]								
	0.1	1	10	0.1	1	10	0.1	1	10
	Mean Cyclic Life Frequency [Cycles/Day]								
	183	1825	18,250	365	3650	36,500	730	7300	73,000
	Relative Reliability Index, R [ppm/°C]								
+20 to +40	2200	790	360	1600	580	270	1150	420	200
+20 to +80	670	240	110	490	170	79	350	130	58
-40 to +40[1]	600	230	110	440	170	83	330	130	62
-40 to 80[1]	370	140	65	270	100	48	200	75	36

(1) These environments straddle the transition region from stress-driven (<20 °C) to strain/creep-driven (>+20 °C); for such environments it has been shown that fatigue occurs significantly earlier by a mechanism different from that underlying this reliability matrix and it should be assumed that the R-values for these environments are optimistic.

7 ppm/°C. Figure 7-2 provides examples of the CTE for some materials used by themselves (polyimide, glass or epoxy glass) and some constraining substrate materials used in conjunction with the printed board dielectric materials.

7.3.2 Thermal Transfer Components, which for thermal reasons require extensive surface contact with the board or with a heatsink mounted on the board, **shall** be compatible with or protected from processing solutions at the conductive interface.

Some thermal transfer mediums need to be assembled in such a fashion as to not be damaged by subsequent assembly operations (i.e., thermal grease, boron nitride, may be damaged or removed by processing operations). Entrapment of processing solutions is also to be avoided.

7.3.3 Thermal Matching A primary thermal concern with through-hole mounted glass components and with ceramic surface-mounted components is the thermal expansion mismatch between the component and the printed board. This mismatch may result in fractured solder joint interconnections if the assembly is subjected to thermal shock, thermal cycling, power cycling and high operating temperatures.

The number of fatigue cycles before solder joint failure is dependent on, but not limited to, the thermal expansion mismatch between the component and the printed board, the temperature excursion over which the assembly must operate, the solder joint size, the size of the component, and the power cycling that may cause an undesirable thermal expansion mismatch if a significant temperature difference exists between the component and the board.

7.4 Thermal Design Reliability Design life can be verified through comparative testing intended to simulate the service environment. Table 7-4 represents an example of design verification of surface mounted devices for three service environments: 0.1 cycles per day, 1 cycle per day, and 10 cycles per day. The service environments shown represent four categories of different temperature ranges. The table establishes a relative reliability index (ppm/°C) for the design depending on a desired equipment life of 5, 10, or 20 years. This reliability index (R) is a factor that may be used in considering if the assembly will survive in the environment for the expected life.

$$R = \Delta\gamma/\Delta T \equiv L_D\,\Delta\alpha/h[\ (ppm/°C)\ ]$$

where:

$\Delta\gamma$ = total solder joint strain (ppm)

ΔT = cyclic temperature swing (°C)

L_D = half the maximum distance between solder joint centers on any component, corner to corner or end to end (mm)

$\Delta\alpha$ = the absolute difference in coefficients of thermal expansion of substrate and component, (ppm/°C)

h = solder joint height (mm)

The longer the life or the more severe the requirements, the lower the number in the matrix becomes. A reliability index roughly gives the maximum cyclic strain that will result in a mean fatigue life just equal to the expected design life. The matrix is primarily meant for leadless components; for leaded components, some underlying relationships are different which, while not changing the indicated trends, will change the matrix quantitatively. Only mean cyclic life is represented, indicating when half the components are expected to fail, not when the first component in a system fails. The statistical distribution of the solder joint fatigue failure has to be included in a reliability assessment.

In the case of through-hole mounted glass components, it is often sufficient to provide stress-relief bends in the component's leads (see section 8.1.14). With surface-mount components, the number of fatigue cycles can be increased by reducing the thermal expansion mismatch, reducing the

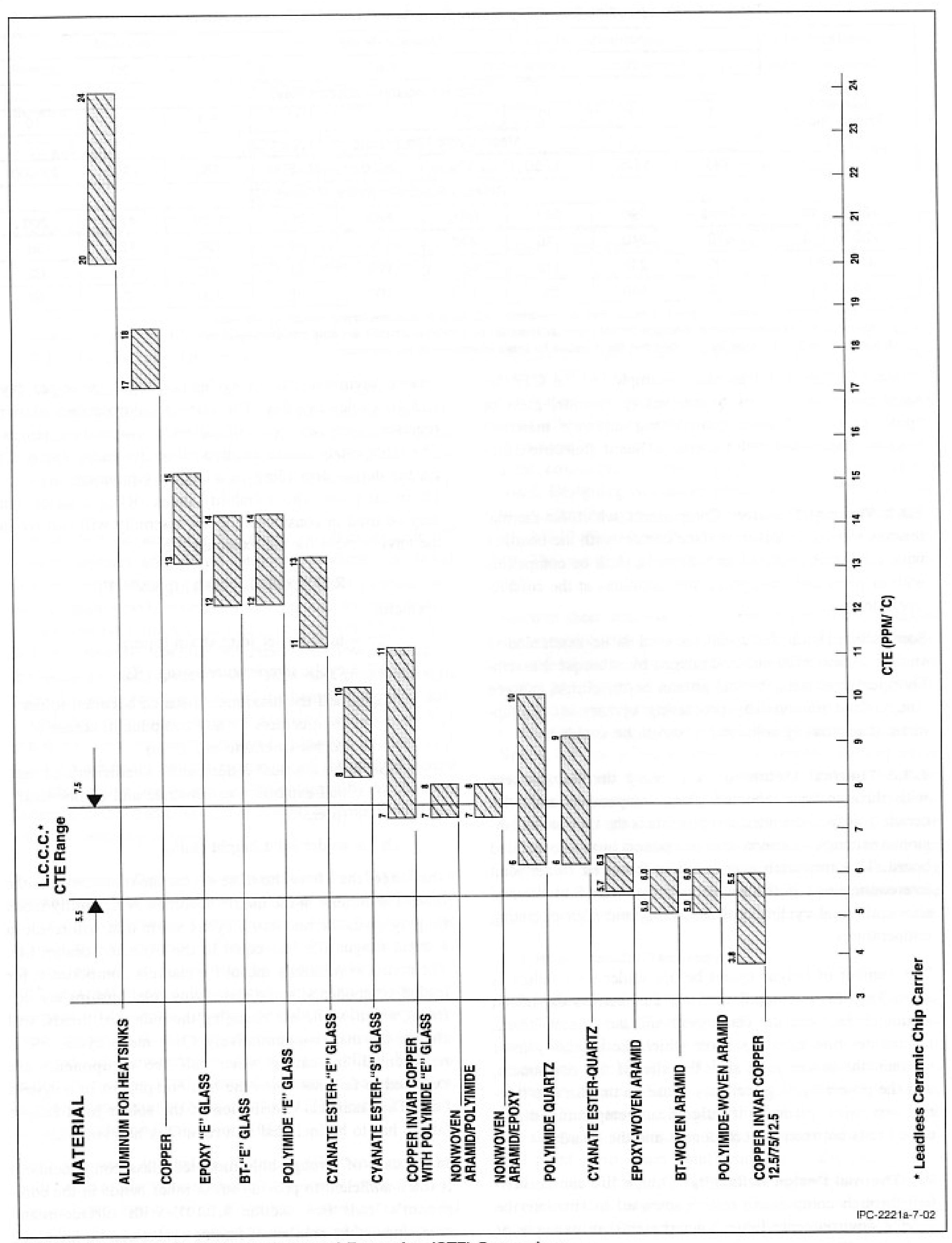


Figure 7-2 Relative Coefficient of Thermal Expansion (CTE) Comparison

temperature gradient, increasing the height of the solder joint, using the smallest physical size component wherever possible, and by optimizing the thermal path between the component and the board. For more detailed information, see IPC-D-279, IPC-SM-785 and IPC-9701.

8 COMPONENT AND ASSEMBLY ISSUES

The mounting and attachment of components play an important role in the design of a printed board. In addition to their obvious effect on component density and conductor routing, these aspects of board design also impact fabrication, assembly, solder joint integrity, repairability and testing. Therefore, it is important that the design reflects appropriate tradeoffs that recognize these and other significant manufacturing considerations.

All components **shall** be selected so as to withstand the vibration, mechanical shock, humidity, temperature cycling, and other environmental conditions the design must endure during installation and subsequently through its entire lifetime usage. The following are requirements the designer should consider and detail on the assembly drawing in specific notes or illustrations.

As a minimum, component mounting and attachment should be based on the following considerations:

- Electrical performance and electrical clearance requirements of the circuit design.
- Environmental requirements.
- Selection of active and passive electronic components and associated hardware.
- Size and weight.
- Minimizing of heat generation and heat dissipation problems.
- Manufacturing, processing and handling requirements.
- Contractual requirements.
- Serviceability requirements.
- Equipment usage and useful life.
- Automatic insertion and placement requirements, when these methods of assembly are to be used.
- Test methods to be employed before, during and after assembly.
- Field repair and maintenance considerations.
- Stress relief.
- Adhesive requirements.

8.1 General Placement Requirements

8.1.1 Automatic Assembly When automatic component insertion and attachment is employed, there are several printed board design parameters that must be taken into account that are not applicable when manual assembly techniques are used.

8.1.1.1 Board Size The size of the printed board to be automatically assembled can vary substantially. Therefore, manufacturers' equipment specifications should be evaluated with respect to the finished board requirements (see 5.3.3).

Standardization of automatic assembly operations can be achieved through standard fixtures that can accommodate a variety of board sizes or assembling boards in panel format. Using the panel assembly concept requires close cooperation with the printed board manufacturer in order to establish tooling concepts, tool hole location, board location, coupon and fiducial locations.

8.1.1.2 Mixed Assemblies Automatic processes used for both surface mounted and through-hole mounted components require special design considerations in order that the components assembled in the first phase of the assembly do not interfere with insertion heads during the second phase.

Component placement **shall** consider the stresses that are put on the board with insertion equipment by isolating parts wherever possible to specific areas such that the second phase insertion/placement stresses do not impact previously soldered connections.

8.1.1.3 Surface Mounting Automatic assembly considerations for surface mounted components include pick-and-place machines used to place/position chip components, discrete chip carriers, small outline packages, and flat packs.

Special orientation symbols should be incorporated into the design to allow for ease of inspection of the assembled surface mounted part. Techniques may include special symbols, or special land configurations to identify such characteristics as a lead of an integrated circuit package.

8.1.2 Component Placement Whenever possible, through-hole parts and components should be mounted on the side of the printed board opposite that which would be in contact with the solder, if the board is machine soldered.

Intermixing of through-hole and surface mount parts, or mounting parts on both sides of the board, requires complete understanding of the assembly and attachment processes (see IPC-CM-770 and IPC-SM-780).

Whenever possible, if their leads are dressed through the holes, axial and nonaxial-leaded components should be mounted per IPC-CM-770 on only one side of the printed board assembly.

Unless a component or part is specifically designed to accept another part into its configuration, there **shall** be no stacking (piggybacking) of components or parts (see J-STD-001).

Component leads **shall** be surface mounted, mounted in through-holes, or mounted to terminals. Lead and wire terminations **shall** be soldered, wire bonded, crimped or compliant pinned.

The variations in the actual placement of the component's leads into plated-through holes or on the termination area in addition to the tolerances on the component's envelope (body and leads) will cause movement of the component body from the intended nominal mounting location. This misregistration **shall** be accounted for such that worst case placement of components **shall** not reduce their spacing to adjacent printed wiring or other conductive elements by more than the minimum required electrical spacing.

If a component is bonded to the surface of the printed board utilizing an adhesive (structural or thermally conductive), the placement of the component **shall** consider the area of adhesive coverage such that the adhesive may be applied without flowing onto or obscuring any of the terminal areas. Part attachment processes **shall** be specified which control the quantity and type of bonding material such that the parts are removable without damage to the printed board assembly. The adhesive used **shall** be compatible with both the printed board material, the component, and any other parts or materials in contact with the adhesive. For some adhesives, contact with adjacent components may not be acceptable. Contact on solder terminations or stress relief areas of adjacent components is another area that is dependent on the material.

Thermal concerns, functional partitioning, electrical concerns, packing density, pick-and-place machine limitations, wave soldering holder concerns, vibration concerns, part interference concerns, ease of manufacture and test, etc., all affect the parts placement.

Parts should be placed on a 0.5 mm [0.020 in] placement grid whenever possible. When a 0.5 mm [0.020 in] grid is not adequate, a 0.05 mm [0.00197 in] placement grid should be used. Certain parts (such as some relays) have leads that are not on standard grids but otherwise the parts should be placed so that the through holes are on grid. Some components, such as TO cans, have leads that are not on grid. In these cases, it is recommended to place the center of the part on grid.

If equipment or other constraints do not allow for a metric grid, parts may be on 2.54 mm [0.100 in] placement grid. When this is not adequate, a 1.27 mm [0.050 in] grid may be used or even a 0.64 mm [0.025 in] grid. The 2.54 mm [0.100 in] placement grid facilitates not only parts insertion but also standard bed-of-nails testing of the board and of the assembly. If bed-of-nails testing is to be used (including in-circuit printed board assembly testing), the test fixturing becomes much more difficult when components are placed off grid.

Figure 7-1 illustrates the producibility design allowances for automatic component insertion. Through hole mount printed boards should observe component to edge of the board spacing constraints on two (2) opposite edges to allow direct insertion into wave solder fingers. Other designs will require fixturing.

Both component heatsink considerations and board heatsink requirements must be addressed in parts placement.

If the printed board assembly will not be tested with a bed-of-nails testing then the assembly grid will be limited only by the assembly machinery. If the printed board assembly is testable with a bed-of-nails scheme, a 2.54 mm [0.100 in] grid for plated through hole spacing is preferred. A 1.91 mm [0.075 in] grid allows greater design density and is not a concern with the assembly machinery but is a concern with bare board and completed assembly testing if a bed-of-nails testing approach is utilized. Bare board testing will normally be done at the printed board supplier and there presently is no cost penalty for off grid nor reduced grid printed board testing.

The designer should allow sufficient component to board edge separation for test and assembly processes. If this is not possible, the designer should consider adding a removable section of board (i.e., breakaway tab). The edge of the component is defined as the physical edge of the component on sides where no leads protrude from the component, and the edge of the surface land pattern for the leaded side of a component. Preferably, components should be a minimum of 1.5 mm [0.0591 in] from the edge of the board and board guide or mounting hardware to allow for component placement, soldering, and test fixturing.

Components should not be grouped in such a way that they shadow one another during soldering. Do not align rows of components perpendicular to the direction of travel; stagger them.

Component polarities should be oriented consistently (in the same direction) throughout a given design.

For wave soldered surface mount chip types, components should be bonded to the printed board prior to automated soldering with an adhesive specially formulated for the purpose.

Specific requirements for part mounting are functions of the type of component, the mounting technology selected for the printed board assembly, the lead bending requirements for the component, the lead stress relief method selected, and placement of the components (either mounted over surfaces without exposed circuitry, over protected surfaces, or over circuitry). Additional requirements are dependent upon the thermal requirements (the operating temperature environment, maximum junction temperature requirements, and the component's dissipated power), and

the mechanical support requirements (based on the weight of the component).

Mounting methods for components of the printed board assembly **shall** be selected so that the final assembly meets applicable vibration, mechanical shock, humidity, and other environmental conditions. The components **shall** be mounted such that the operating temperature of the component does not reduce the component's life below required design limits. The selected component mounting technique **shall** ensure that the maximum allowable temperature of the board material is not exceeded under operating conditions.

8.1.3 Orientation Components should be mounted parallel to the edges of the printed board. They should also be mounted parallel or perpendicular to one another in order to present an orderly appearance. When appropriate, the component should be mounted in such a manner as to optimize the flow of cooling air.

Assemblies are usually flow soldered with the top edge of the board in the lead (perpendicular to the direction of travel through the wave), mounting flanges and hardware against the fixture or conveyor fingers, and edge connector last. Surface mount components should be placed to facilitate solder flow in the wave. Rectangular components (with solder caps at the ends) should be oriented with the long axis parallel to the leading edge of the board, perpendicular to the direction of travel. This avoids the "shadow" effect, where the body of the component would otherwise prevent free flow of solder to the trailing solder joint (see Figure 8-1).

8.1.4 Accessibility Electronic components **shall** be located and spaced so that the lands for each component are not obscured by any other component, or by any other permanently installed parts. Each component **shall** be capable of being removed from the assembly without having to remove any other component. These requirements do not apply to assemblies manufactured with no intent to repair (throw away assemblies) or as specified in 8.2.13.

8.1.5 Design Envelope The projection of the component, other than connectors on the board should not extend over the edge of the board or interfere with board mounting.

Unless otherwise detailed on the assembly drawing, the board edge is regarded as the extreme perimeter of the assembly, beyond which no portion of the component, other than connector, is allowed to extend. The designer **shall** prescribe the perimeter with due regard for maximum part body dimensions and the mounting provisions dictated by the board and assembly documentation.

8.1.6 Component Body Centering Except as otherwise specified herein, the bodies (including end seals or welds) of horizontally mounted, axial leaded components should be approximately centered in the span between mounting holes, as shown in Figure 8-2.

8.1.7 Mounting Over Conductive Areas Metal-cased components **shall** be mounted so that they are insulated from adjacent electrically conductive elements. Insulation materials **shall** be compatible with the circuit and printed board material.

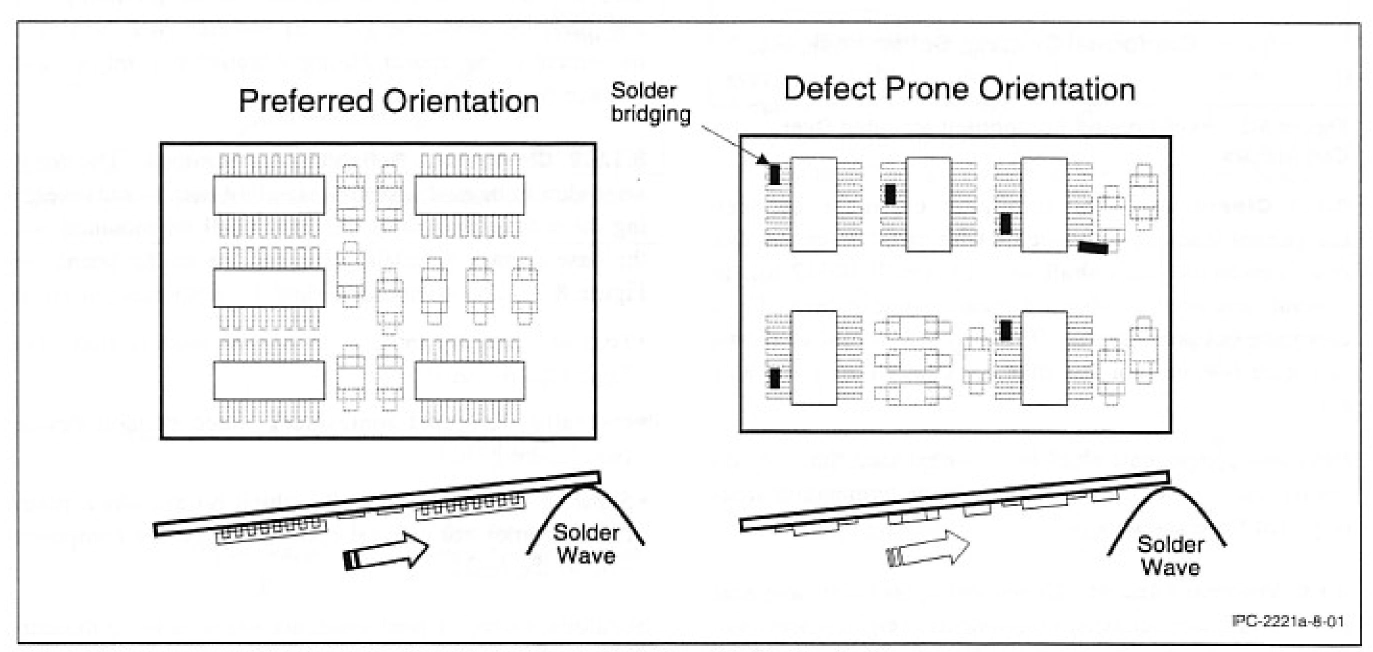


Figure 8-1 Component Orientation for Boundaries and/or Wave Solder Applications

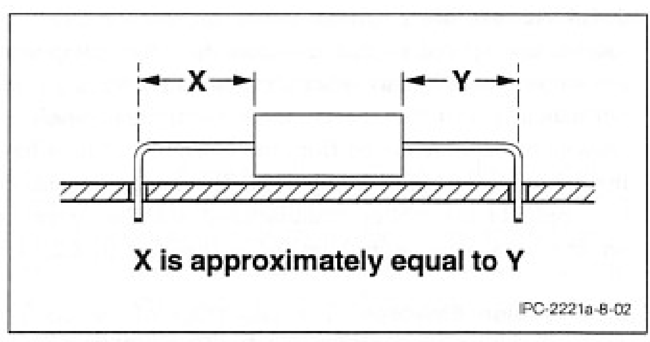


Figure 8-2 Component Body Centering

Conductive areas under the parts **shall** be protected against moisture entrapment by one of the following methods.

- Application of conformal coating using material in accordance with IPC-CC-830 (usually specified on the assembly drawing).
- Application of cured resin coating by using low flow prepreg material.
- Application of a permanent polymer coating (solder resist) using material in accordance with IPC-SM-840.

This requirement is applicable to components with or without sleeving (see Figure 8-3).

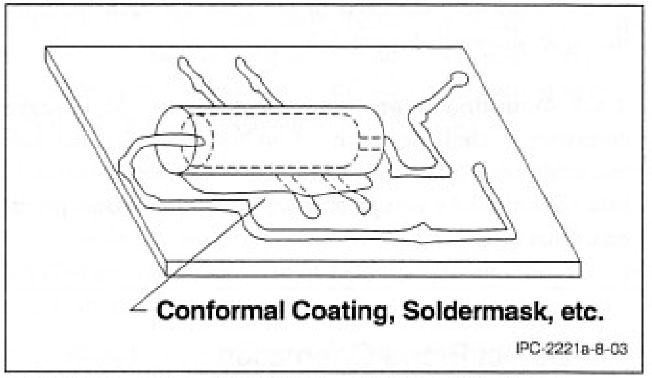


Figure 8-3 Axial-Leaded Component Mounted Over Conductors

8.1.8 Clearances The minimum clearance between component leads or components with metal cases and any other conductive path **shall** be 0.13 mm [0.00512 in]. In general, uncoated conducting areas should provide for a clearance of approximately 0.75 mm [0.0295 in] as shown in Figure 8-4, but not less than the values shown in Table 6-1.

Parts and components **shall** be mounted such that they do not obstruct solder flow onto the topside termination areas of plated through-holes.

8.1.9 Physical Support Dependent upon weight and heat generation characteristics, components weighing less than 5 grams per lead which dissipate less than 1 watt, and are not clamped or otherwise supported **shall** be mounted with the component body in intimate contact with the printed board if practical, unless otherwise specified.

8.1.9.1 Component Mounting Techniques for Shock and Vibration The design stage should be such that axial-leaded components weighing less than 5 grams per lead **shall** be mounted with their bodies in intimate contact with the board. Dimensional criteria for lead bending and spacing **shall** be as specified in Figure 8-9. Axial-leaded components weighing 5 grams or more per lead should be secured to the board utilizing mounting clamps. If clamps are not practical due to density considerations, other techniques should be employed such that the solder connections are not the only means of mechanical support. These techniques are used for components weighing more than 5 grams when high vibration requirements must be met (see 5.2.7 and Figures 8-5 and 8-6).

When mounting chip components on edge, if the vertical dimension is greater than the thickness dimension, then chip components should not be used in assemblies subject to high vibration or shock loads. Vertical mounting **shall** be used for:

a) Low and tall profile SMDs with reflow termination pads located in a single base surface.

b) Nonaxial-leaded devices with leads egressing from two or more sides of the device(s).

c) Nonaxial-leaded devices with leads egressing from a single base surface.

For radial leaded components with three or more leads, such as transistors, that require the use of spacers between their base and the board surface for vertical mounting, special attention should be given to ensuring that there is no movement of the spacer during vibration that might cause damage to surface conductors.

8.1.9.2 Class 3 High Reliability Applications The design stage should be such that free standing components weighing more than 5.0 grams per lead **shall** be mounted with the base surface paralleling the surface of the board (see Figure 8-7). The component **shall** be supported on either:

- Feet or standoffs integral to the component body (see Figure 8-7A and B).
- Specially configured nonresilient footed standoff devices (see Figure 8-7C).
- Separate nonfooted standoffs which do not block plated through-holes nor conceal connections on the component side of the board.

Standoffs, footed or nonfooted, are intended to be mounted flush to the surface of the board. For this requirement, a button standoff as shown in Figure 8-7B is considered a

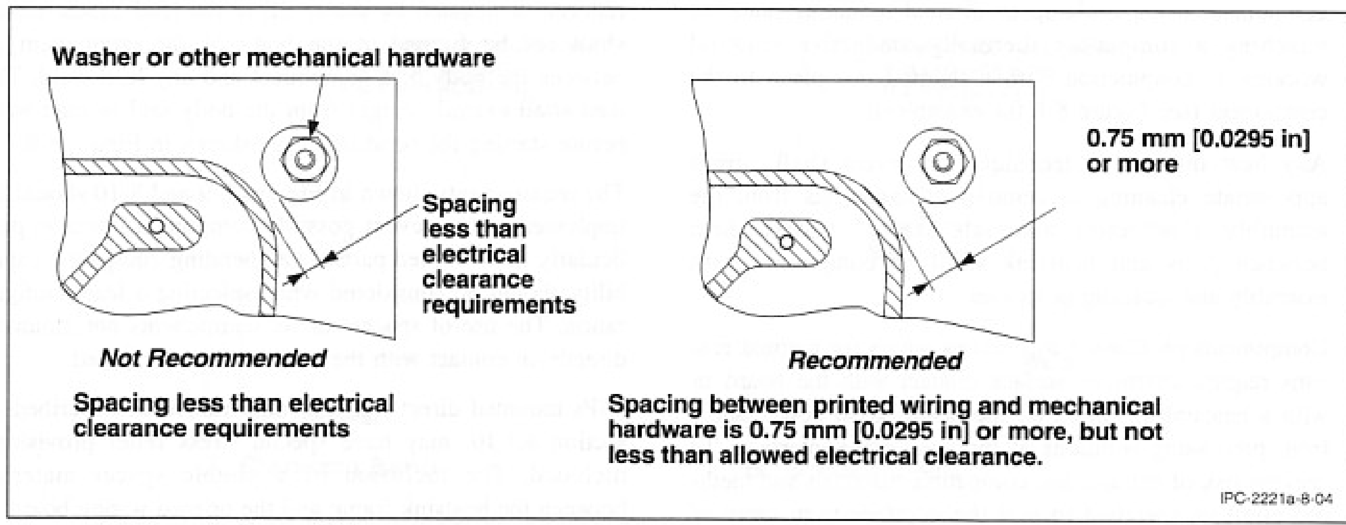


Figure 8-4 Uncoated Board Clearance

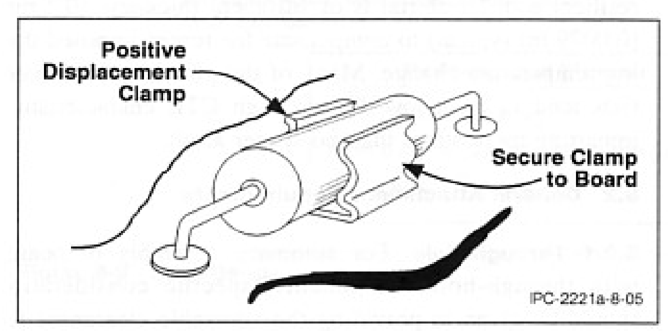


Figure 8-5 Clamp-Mounted Axial-Leaded Component

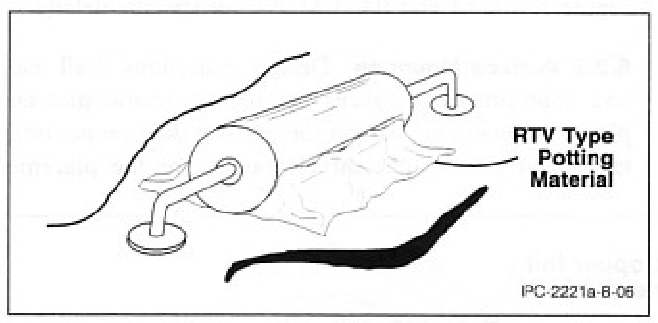


Figure 8-6 Adhesive-Bonded Axial-Leaded Component

foot. Footed standoffs, as illustrated in Figures 8-7C and 8-7D, **shall** have a minimum foot height of 0.25 mm [0.00984 in].

When a separate footed standoff device or separate base nonfooted standoff is utilized and the component is mounted with the base surface paralleling the board surface, mounting should be such that the component base is seated in contact with, and flat to, the footed or nonfooted standoff. Mounting should also be such that the feet of the footed standoff maintain full contact with the board surface. No standoff **shall** be inverted, tilted, or canted, and should not be seated with any foot (or base surface) out of contact with the board or conductors thereon. Neither **shall** the component be tilted, canted nor separated from the mating surface of the resilient standoff device.

8.1.10 Heat Dissipation Design for heat dissipation of components **shall** insure that the maximum allowable temperature of the board material and the component is not exceeded under operating conditions. Heat dissipation may be accomplished by requiring a gap between board and

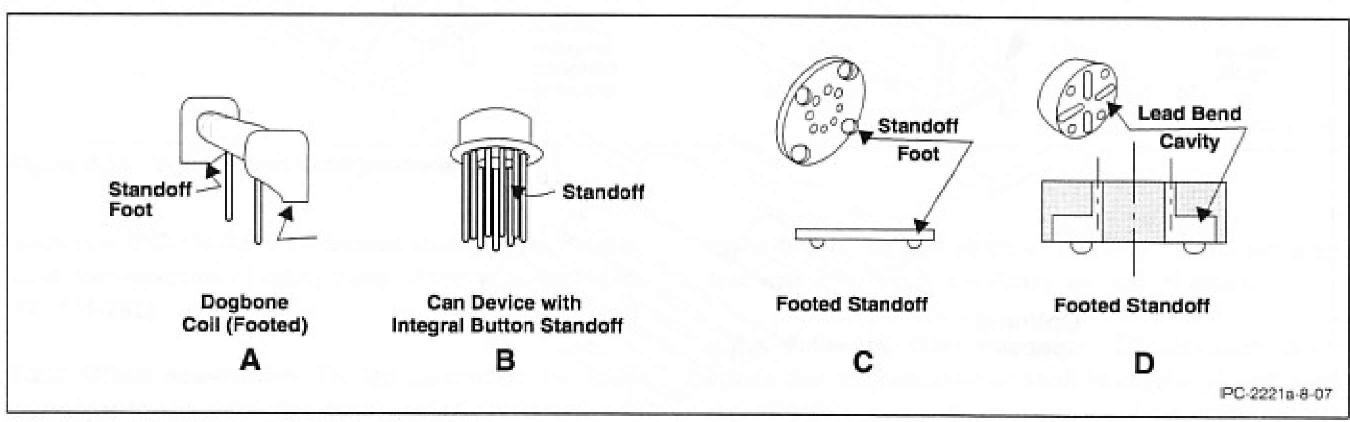


Figure 8-7 Mounting with Feet or Standoffs

component, using a clamp or thermal mounting plate, or attaching a compatible thermally-conductive material working in conjunction with a thermal bus plane to the component (see Figure 8-8 for examples).

Any heat dissipation technique or device **shall** permit appropriate cleaning to remove contaminants from the assembly. Conductive materials used to transfer heat between parts and heatsink **shall** be compatible with assembly and cleaning processes.

Components on Class 3 assemblies which for thermal reasons require extensive surface contact with the board or with a heatsink mounted on the board, **shall** be protected from processing solutions at the conductive interface. To prevent risk of entrapment, compatible materials and methods **shall** be specified to seal the interface from entry of corrosive or conductive contaminants.

Note: Even totally nonmetallic interfaces that are prone to entrap fluids can have adverse effects on the fabricator's ability to pass required cleanliness tests.

8.1.11 Stress Relief When designing for stress relief, lands and terminals **shall** be located by design so that components can be mounted or provided with stress relief bends in such a manner that the leads cannot overstress the part lead interface when subjected to the anticipated environments of temperature, vibration, and shock. Where the lead bend radius cannot be in accordance with Figure 8-9 in order to achieve design goals, the bends **shall** be detailed on the assembly drawing.

The leads of components mounted horizontally with their bodies in direct contact with the printed board **shall** be mounted with a method that ensures that stress relief is not reduced or negated by solder fill in the lead bends. Leads **shall** not be formed at the body of the component or between the body of a component and any lead weld. The lead **shall** extend straight from the body seal or lead weld before starting the bend radius as shown in Figure 8-9.

The requirements shown in Figures 8-9 and 8-10 should be implemented to prevent possible component damage, particularly glass-bodied parts. Lead bending equipment capability should be considered when selecting a lead configuration. The use of spacers under components not mounted directly in contact with the board is recommended.

DIPs mounted directly to heatsink frames, as described in section 8.1.10, may have special stress relief provisions included. The inclusion of a pliable spacer material between the heatsink frame and the printed wiring board is an acceptable method for ensuring stress relief provided the resilient added material is of sufficient thickness (0.2 mm [0.0079 in] typical) to compensate for forces imposed during temperature change. Many of the pliable spacer materials tend to have low T_g and high CTE characteristics, imparting more stress than no spacer at all.

8.2 General Attachment Requirements

8.2.1 Through-Hole For automatic assembly of boards with through-hole components, specific consideration should be given to providing the allowable clearances for the insertion and clinching of leads of the components. See Figure 7-1, 8.3.1 and IPC-CM-770 for specific details.

8.2.2 Surface Mounting Design restrictions **shall** maintain appropriate clearances for the automatic pick-and-place equipment to position the parts in their proper orientation and allow sufficient clearances for the placement

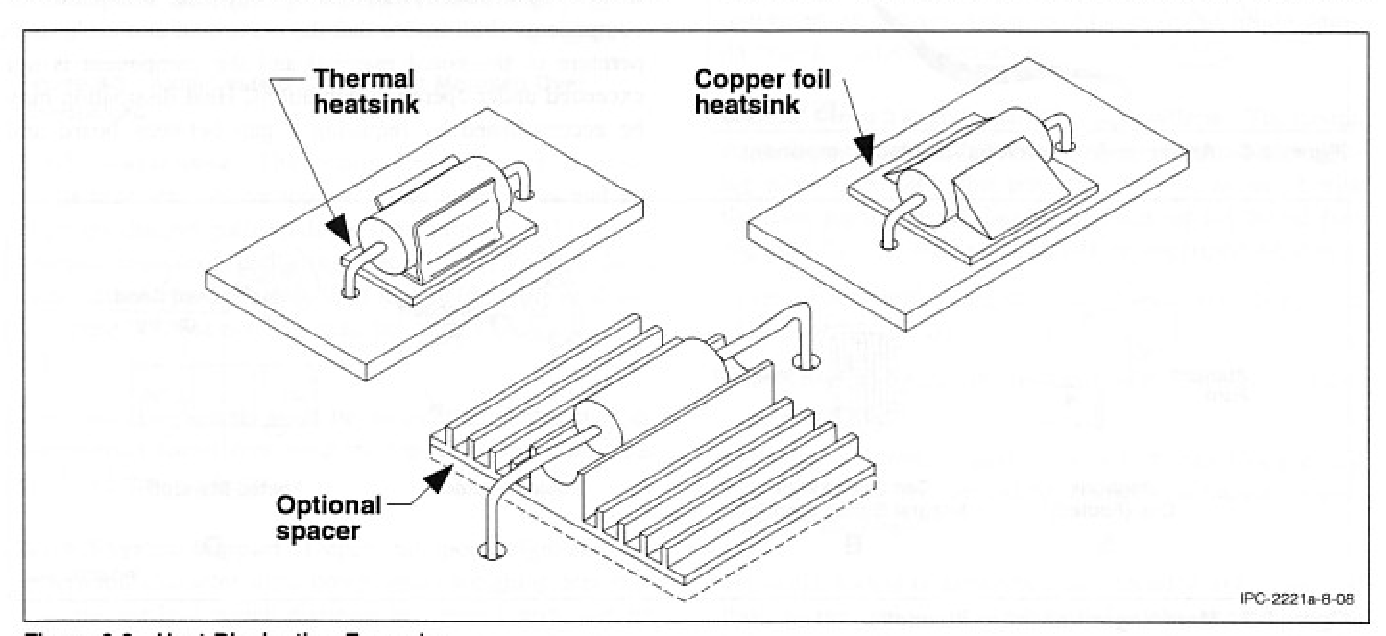
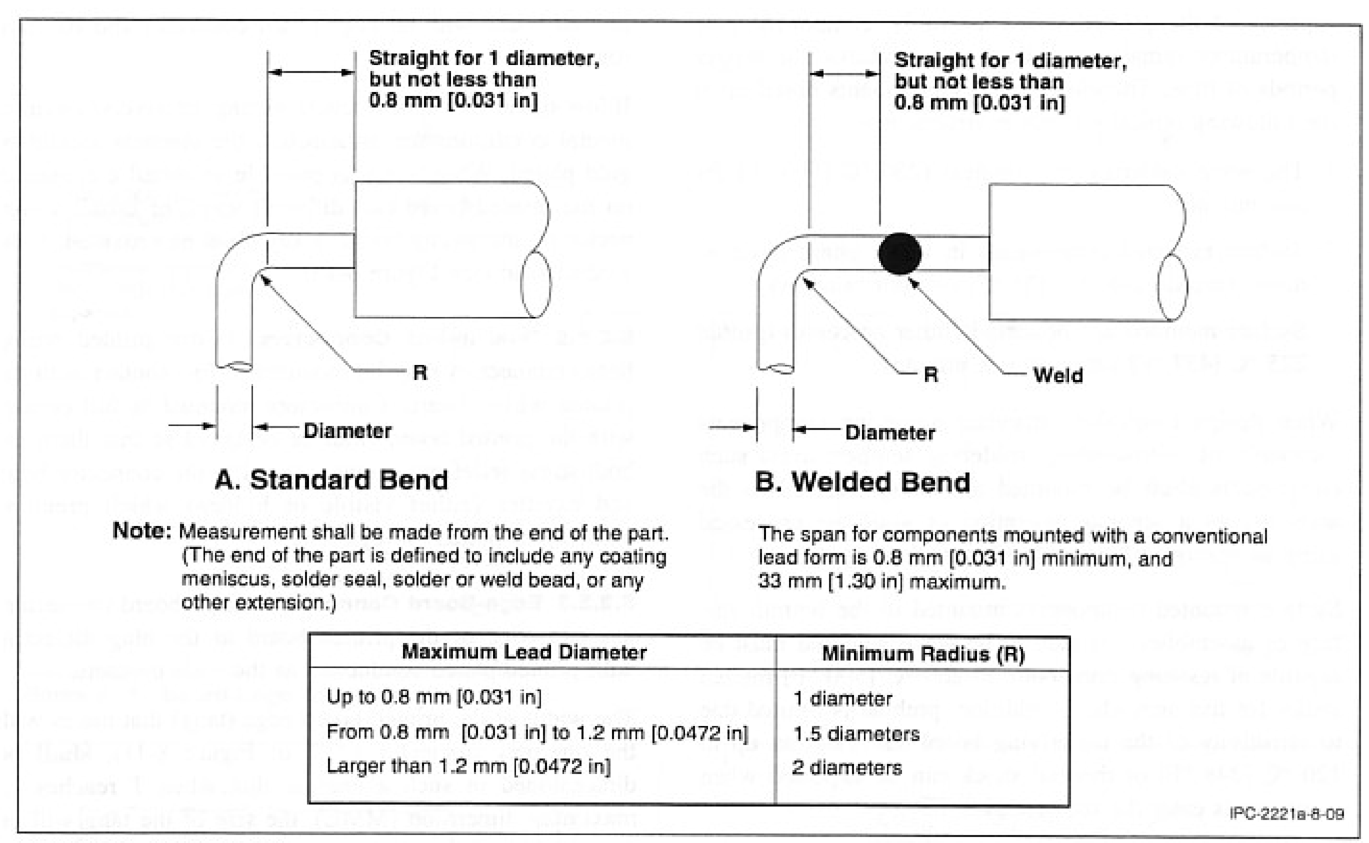


Figure 8-8 Heat Dissipation Examples



Maximum Lead Diameter	Minimum Radius (R)
Up to 0.8 mm [0.031 in]	1 diameter
From 0.8 mm [0.031 in] to 1.2 mm [0.0472 in]	1.5 diameters
Larger than 1.2 mm [0.0472 in]	2 diameters

Figure 8-9 Lead Bends

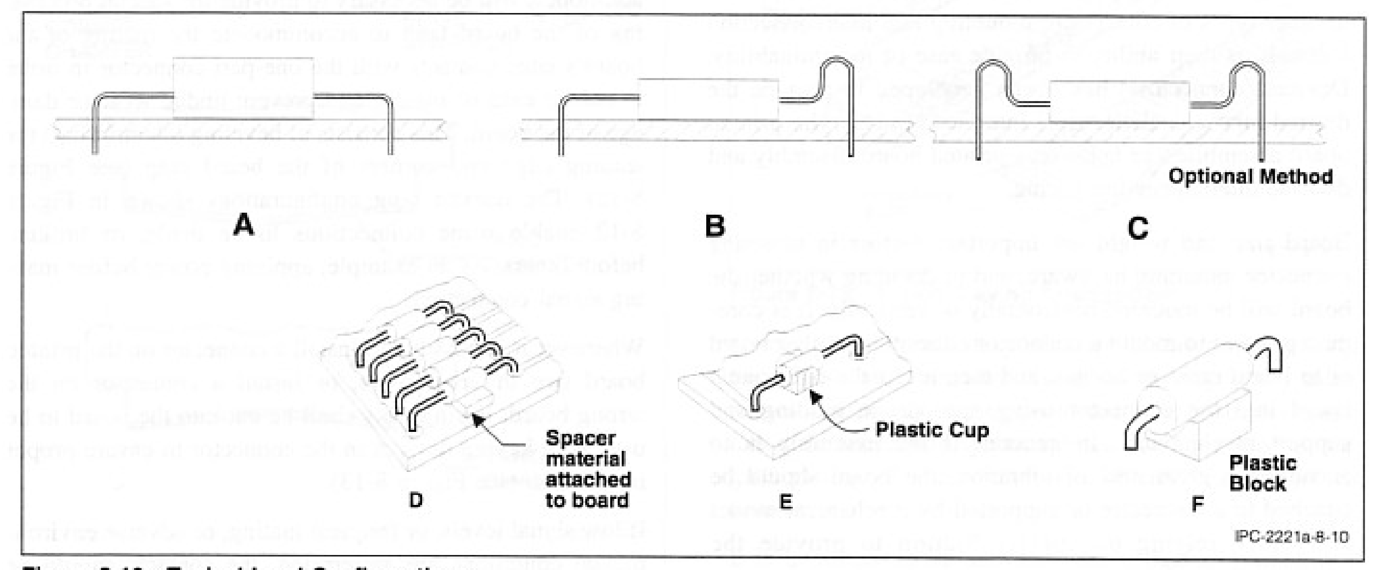


Figure 8-10 Typical Lead Configurations

heads (see IPC-SM-780). Clearances should be provided to allow for inspection of solder joints wherever possible (see IPC-SM-782).

8.2.3 Mixed Assemblies Design parameters for automatic processes used for both surface mounted and through-the-board mounted components require special design considerations in order that the components assembled in the first phase of the assembly do not interfere with insertion heads during the second phase.

8.2.4 Soldering Considerations The designer should ensure that components used **shall** be capable of withstanding soldering temperatures used in the assembly process. Although the components are exposed to these temperatures for relatively short periods of time, due to the thermal

capacity of the printed board assembly, component case temperatures remain near these temperatures for longer periods of time. Therefore, select components based upon the following typical process environments:

1. The wave soldering environment (260 °C [500 °F] for one minute).
2. Surface mounted components in vapor phase environments (profile 216 °C [421 °F] for four minutes).
3. Surface mounted components in other processes (profile 225 °C [437 °F] for up to one minute).

When design restrictions mandate mounting components incapable of withstanding soldering temperatures, such components **shall** be mounted and hand-soldered to the assembly as a separate operation or **shall** be processed using an approved localized reflow technology.

Surface mounted components mounted to the bottom surface of assemblies intended to be wave soldered must be capable of resisting immersion in 260 °C [500 °F] molten solder for five seconds. In addition, preheat is limited due to sensitivity of the underlying board substrate, so up to 120 °C [248 °F] of thermal shock can be expected when components enter the solder wave.

8.2.5 Connectors and Interconnects One of the major advantages of using printed board assemblies, as opposed to other types of component mounting and interconnection methods, is their ability to provide ease of maintainability. Devices (connectors) have been developed to provide the desired mechanical/electrical interface between the printed board assemblies, or between a printed board assembly and discrete interconnection wiring.

Board size and weight are important factors in choosing connector mounting hardware, and in deciding whether the board will be mounted horizontally or vertically. It is common practice to mount a connector either to a mother board or to board racks or frames, and then insert the component board into the connector using appropriate guiding and support mechanisms. In general, if the assembly is to encounter a great deal of vibration, the board should be attached to a connector or supported by mechanical means other than relying on contact friction to provide the mechanical interface.

Connectors may be mounted to the printed board by soldering, welding, crimping, press fitting or other means. Leads may be extended through holes or contact may be made to lands provided on the board. Holes may be plated through or simply drilled. The exact method will depend on the connector design.

8.2.5.1 One-Part Connectors One part connectors provide the female receptacle for communication between the printed board with an edge-board connector and its environment.

If low signal levels, or frequent mating, or adverse environmental conditions are anticipated, the contacts should be gold plated. Whenever it is possible to install a connector on the printed board two different ways, or install a connector on the wrong board, a key **shall** be provided in the contact field (see Figure 8-13).

8.2.5.2 Dual In-line Connectors In-line printed wiring board connectors may be mounted in full contact with the printed wiring board. Connectors mounted in full contact with the printed board **shall** be designed so that there are both stress relief provisions internal to the connector body and cavities (either visible or hidden) which preclude blocking of plated through-holes.

8.2.5.3 Edge-Board Connectors Edge-board connectors use one edge of the printed board as the plug dielectric with printed/plated conductors as the male contacts.

The width of the printed board edge (tang) that mates with the one-part connector ("T" of Figure 8-11), **shall** be dimensioned in such a manner that when T reaches its maximum dimension (MMC), the size of the tang will be no greater than the minimum throat of the one-part connector. (See 5.4.3 for establishing connector circuit pattern.) In addition, it will be necessary to provide for special processing of the board tang to accommodate the mating of the board's edge contacts with the one-part connector in order to permit ease of mating and prevent undue wear or damage of the board. This consists of beveling (chamfering) the leading edge and corners of the board tang (see Figure 8-12). The uneven tang configurations shown in Figure 8-12 enable some connections to be made, or broken, before others. As an example, applying power before making signal connections.

Whenever it is possible to install a connector on the printed board two different ways, or install a connector on the wrong board, keying slots **shall** be cut into the board to be used with keying devices in the connector to ensure proper installation (see Figure 8-13).

If low signal levels, or frequent mating, or adverse environmental conditions are anticipated, the contacts should be gold-plated.

8.2.5.4 Two-Part Multiple Connectors Two-part multiple connectors consist of self-contained multiple contact plug and receptacle assemblies. Usually, although not always, the receptacle is an unmoveable connector assembly which mounts to an interconnection-wiring backplane (motherboard) or chassis (see Figure 8-14). Each connector half may have either male or female contacts. For safety, the receptacle usually contains female power contacts.

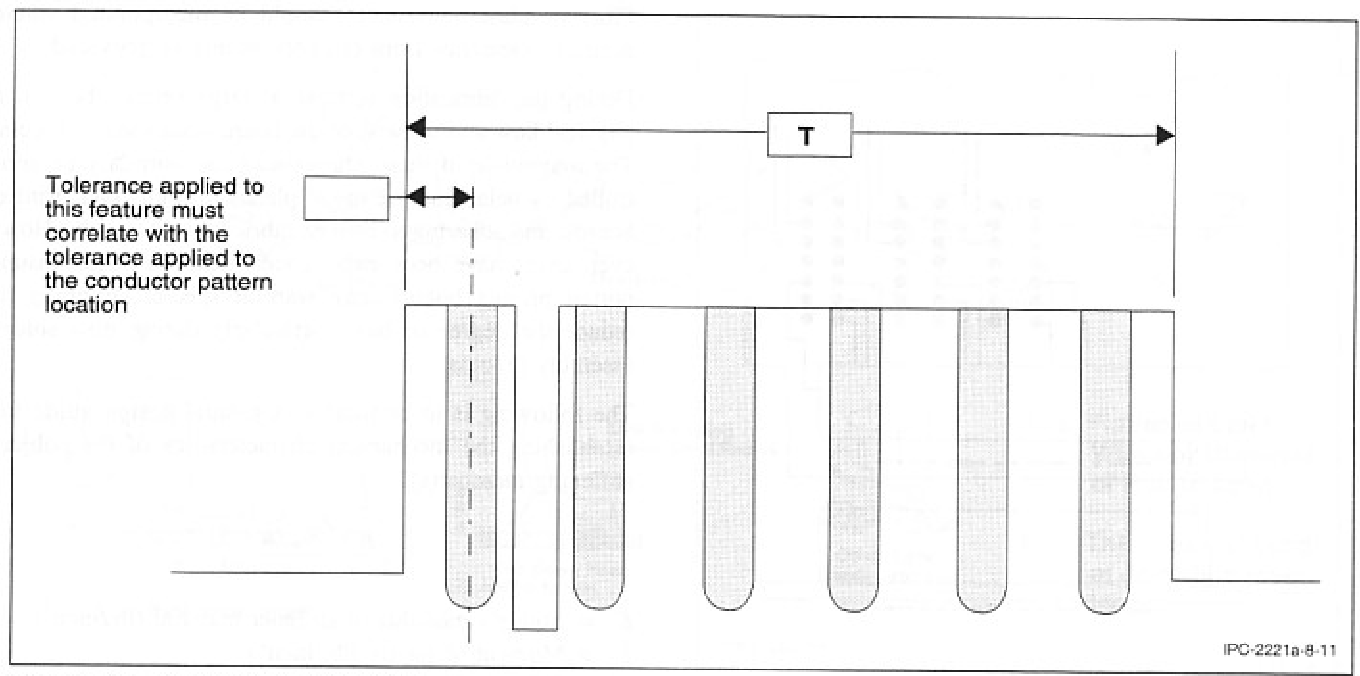


Figure 8-11 Board Edge Tolerancing

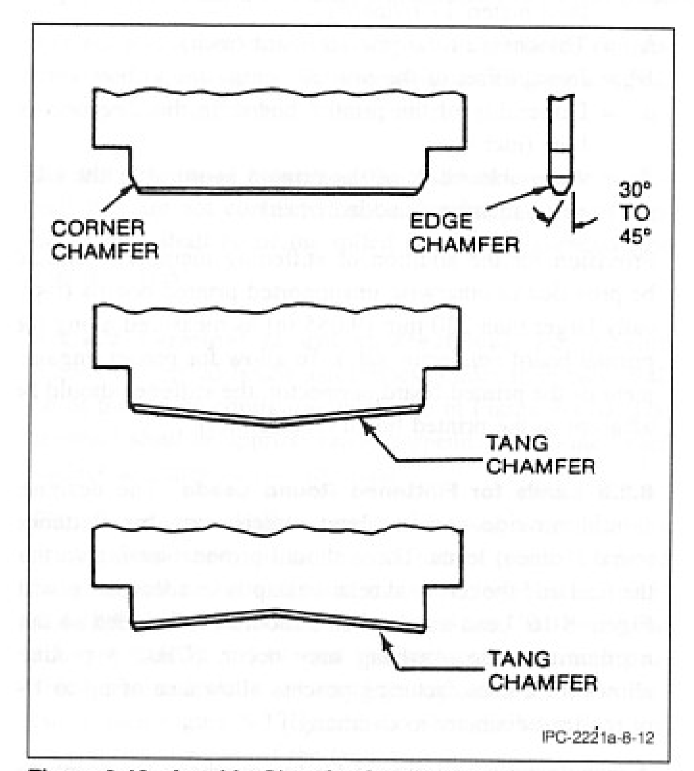


Figure 8-12 Lead-In Chamfer Configuration

8.2.5.5 Two-Part Discrete-Contact Connectors Two-part discrete-contact connectors that consist of individual plug (male), and receptacle (female) contacts are mounted directly to the printed board, usually without being part of molded dielectric assemblies.

8.2.5.6 Edge-Board Adapter Connectors Edge-board adapter connectors may be used in lieu of printed/plated conductors as the male contacts (see Figure 8-15). These

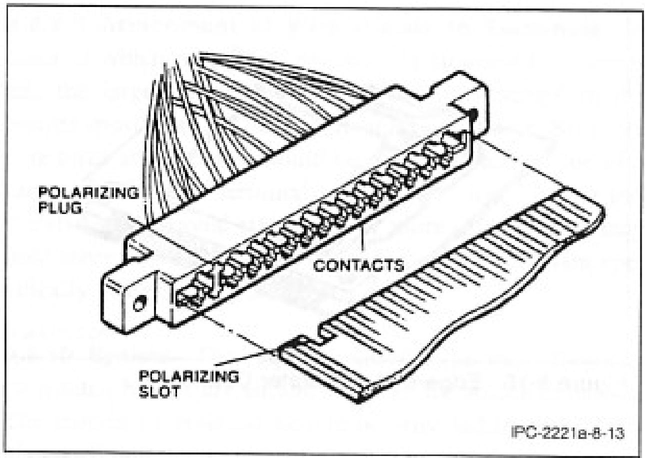


Figure 8-13 Typical Keying Arrangement

connectors eliminate many of the problems associated with the edge-board connectors, such as varying board thicknesses and board warping problems. Use of these connectors does not require special printed board processing, e.g., gold plating of contacts or tang chamfer on the printed board.

It is important to be sure that the method of mounting is sufficiently strong to withstand the forces of mating and withdrawal.

When one part of the connector is mounted to a printed board backplane using press-fit technology, the backplane should be designed in accordance with the guidelines of IPC-D-422.

8.2.6 Fastening Hardware The installed location and installation orientation for fastening hardware **shall** be prescribed on the assembly drawing for such devices as rivets,

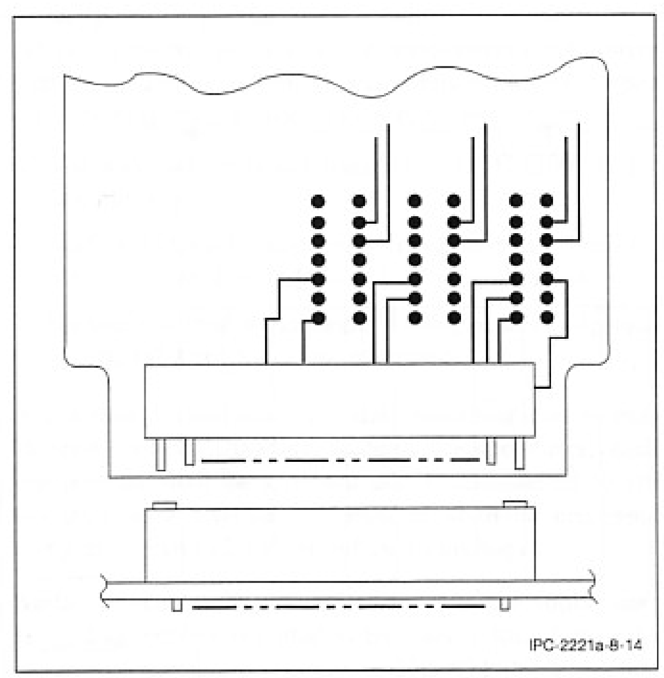


Figure 8-14 Two-Part Connector

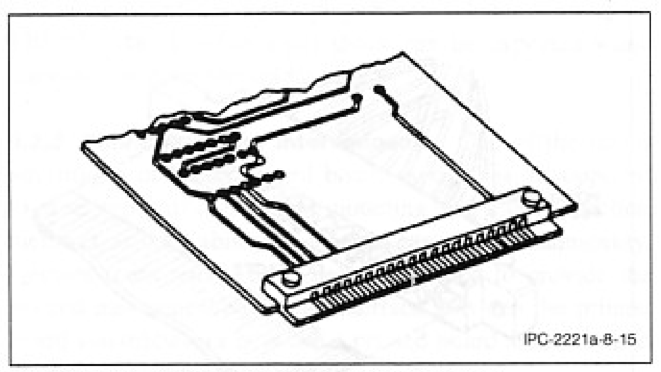


Figure 8-15 Edge-Board Adapter Connector

machine screws, washers, inserts, nuts and bracketry. Specifications and precautions of tightening torques **shall** be provided wherever general assembly practice might be inadequate or detrimental to the assembly's structure or functioning. The use of such hardware should be in accordance with the clearance requirements of this section.

8.2.7 Stiffeners Stiffeners are designed into the board to provide rigidity to the assembly and prevent flexing of the circuitry which could cause solder and copper foil cracking during mechanical stress.

Stiffeners may be fabricated from aluminum, steel having an adequate protective finish, plastic or fiber reinforced material. Stiffeners may be attached to the board with solder or by fasteners (rivets, nuts and bolts). If the stiffener is soldered using flow solder process, the board typically must be held flat by flow solder fixtures.

Adequate physical and electrical clearance must be provided between stiffeners, conductors, and components. Fiber or plastic insulators should be incorporated where adequate clearance from circuitry cannot be provided.

During the fabrication process of large printed boards, a physical bow and/or twist of the board occasionally occurs. The magnitude of these phenomena can normally be controlled by balancing the metal planes in multilayer printed boards, and adhering to proven fabrication processes. However, cases have been experienced whereby large unsupported printed boards may warrant special stiffening to reduce the degree of bow particularly during flow solder assembly process.

The following is to be used as a general design guide for establishing the mechanical characteristics of the subject stiffening member(s).

$$E = \frac{E^1 h^3}{I} \frac{W_o (a+5)}{300Z}$$

E = Young's modulus of stiffener material (lb./inch^2)
I = Moment of inertia (lb. inch^2)
E^I = Flexural modulus of elasticity of the printed board base material (lb./inch^2)
h = Thickness of the printed board (inch)
W_o = Initial offset of the printed board, due to bow (inch)
a = Dimension of the printed board, in the direction of bow (inch)
Z = Allowable offset of the printed board after the stiffening member is added (inch)

Provision for the addition of stiffening member(s) should be provided to otherwise unsupported printed boards (typically larger than 230 mm [9.055 in] as measured along the printed board connector side). To allow for proper engagement of the printed board connector, the stiffener should be adjacent to the printed board connector(s).

8.2.8 Lands for Flattened Round Leads The designer should provide specific land attachments for flattened round (coined) leads. These should provide seating so that the heel and the terminal relationship is in accordance with Figure 8-16. Lead and land size should be designed so that a minimum side overhang may occur. (Class 3 product allows for a manufacturing process allowance of up to 1/4 of the lead diameter to overhang.)

A manufacturing allowance for toe overhang is acceptable provided it does not violate the minimum designed conductor spacing. If flattened leads are used, the flattened thickness **shall** not be less than 40% of the original diameter (see J-STD-001).

8.2.9 Solder Terminals Single-/double-ended, or single-/multisectioned turret solder terminals may be used to facilitate the installation of components, jumper wires, input/output wiring, etc. The wires or leads of components **shall** be soldered to the posts of the solder terminals.

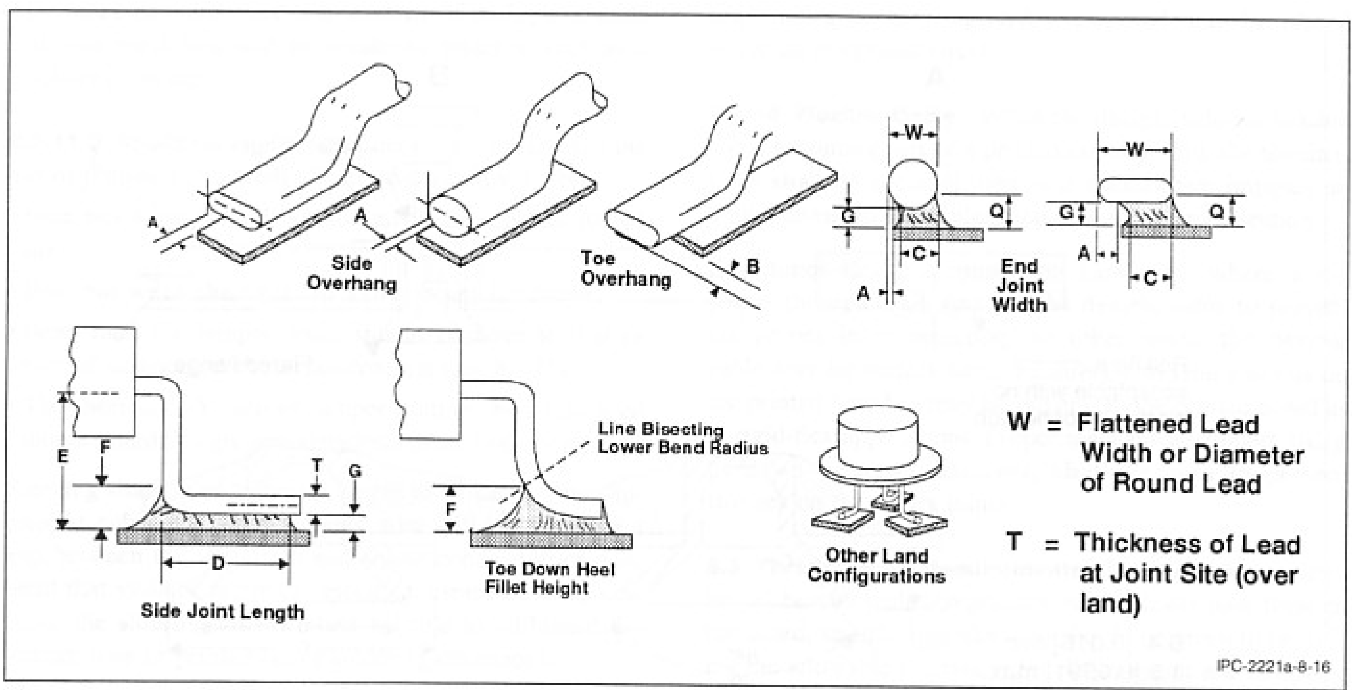


Figure 8-16 Round or Flattened (Coined) Lead Joint Description

Eyelets and solder terminals are to be considered components and specified on the assembly drawing or a subassembly drawing for board fabrication.

8.2.9.1 Terminal Mounting-Mechanical Solder terminals that are not connected to conductive patterns or copper planes **shall** be of the rolled flange configuration (see Figure 8-17A).

8.2.9.2 Terminal Mounting-Electrical For printed boards or printed board assemblies, solder terminals **shall** be of the flange configuration shown in Figure 8-17B. The terminal **shall** be approximately perpendicular to the board surface and may be free to rotate.

Flat body flanges **shall** be seated to the base material of the printed board and not on ground planes or lands. Flared flanges **shall** be formed to an included angle between 35° and 120° and **shall** extend between 0.4 mm [0.016 in] and 1.5 mm [0.0591 in] beyond the surface of the land provided minimal electrical spacing requirements are maintained (see Figure 8-17B) and the flare diameter does not exceed the diameter of the land.

Terminals should only be mounted in unsupported holes or in plated-through holes in Type 2 boards with a nonfunctional land on the component side (see Figure 8-17B). If it is essential that a terminal be utilized for interfacial connection, on Type 3 through Type 6 (inclusive) boards, a dual hole configuration incorporating a supported plated-through hole **shall** be combined with the terminal hole interconnected by a land on the solder side of the printed board (see Figure 8-18).

8.2.9.3 Attachment of Wires/Leads to Terminals In cases in which more than one wire is attached to a terminal, the largest diameter wire should be mounted to the bottom-most post for ease of rework and repair. No more than three attachments should be made to each section of a turret of bifurcated terminal. As an exception, bus bar terminals (see sectional standards for more information) may hold more than three wires or leads per section when specifically designed to hold more.

8.2.10 Eyelets The requirements for the use of eyelets on printed boards are similar to those for solder terminals. The criteria for their use should be provided by the assembly drawing.

Interfacial connections **shall** not be made with eyelets. Eyelets installed at an electrically functional land **shall** be required to be of the funnel flange type.

8.2.11 Special Wiring

8.2.11.1 Jumper Wires It may be necessary to include point-to-point wiring to a printed board as a part of the original design. Such wiring **shall** not be considered as being part of the printed board, but as part of the board assembly process, and considered as components. Therefore, their use **shall** be documented on the printed board assembly drawing.

Jumper wires **shall** be terminated in holes, on lands or standoffs. Jumper wires **shall** not be applied over or under other replaceable components (including uninsulated jumper wires).

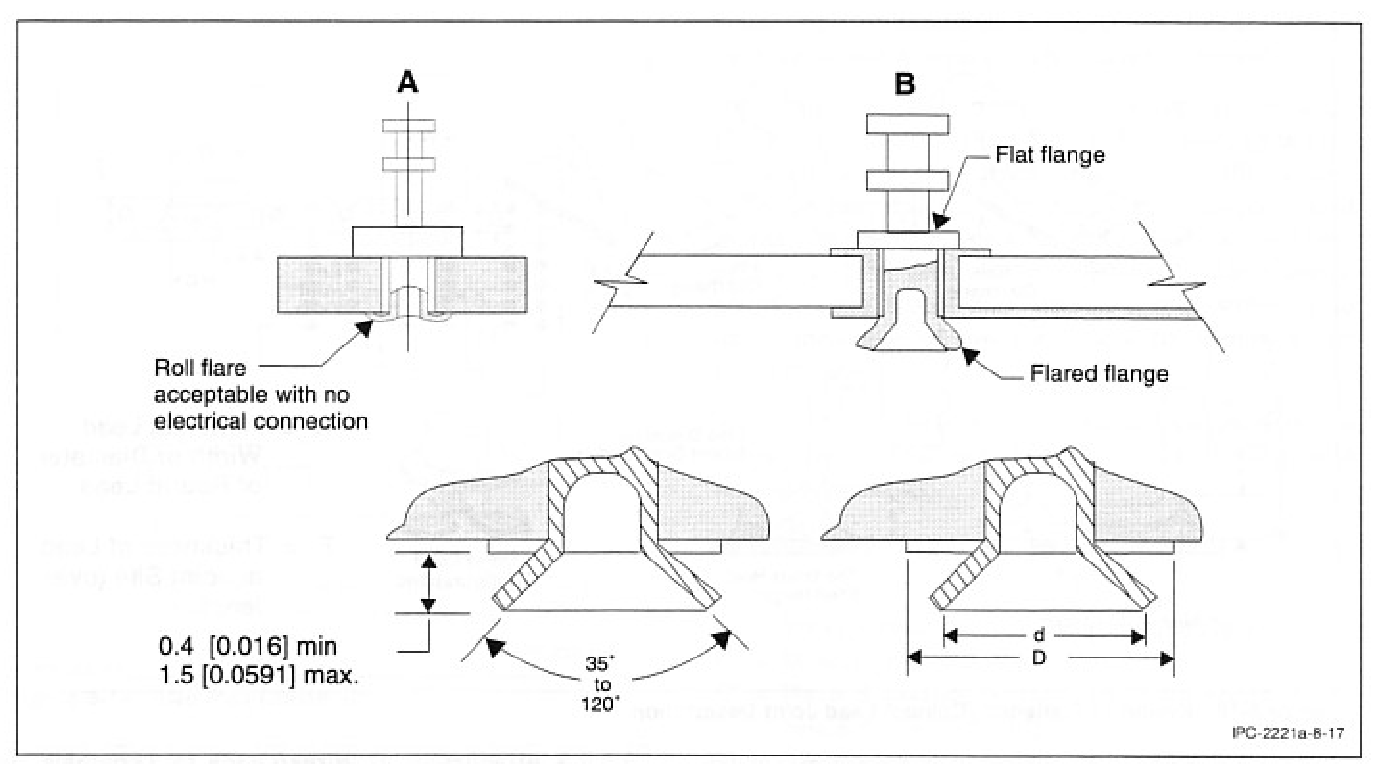


Figure 8-17 Standoff Terminal Mounting, mm [in]

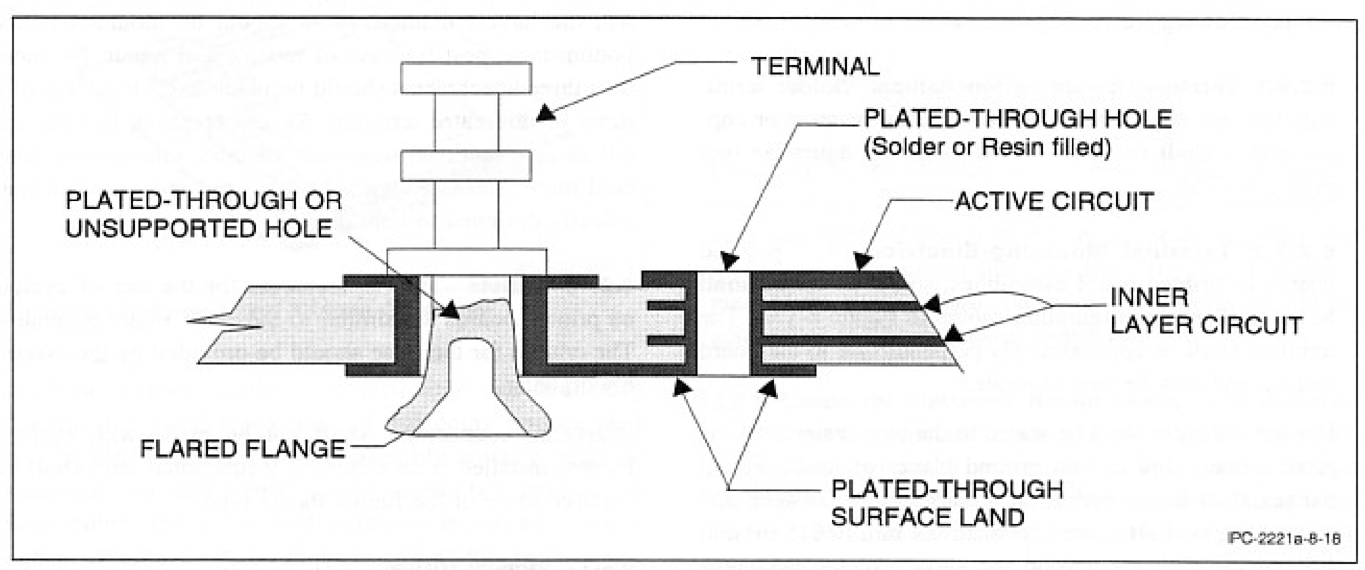


Figure 8-18 Dual Hole Configuration for Interfacial and Interlayer Terminal Mountings

Jumper wires **shall** be permanently fixed to the printed board at intervals not to exceed 25 mm [0.984 in]. Jumper wires less than 25 mm [0.984 in] length whose path does not pass over conductive areas and does not violate the spacing requirements may be uninsulated. Insulation, when required on jumper wires, **shall** be compatible with the use of any conformal coatings. When using nonsealed wire insulation, consider the assembly cleaning process.

8.2.11.2 Types Point-to-point (jumper) wires are usually of the following types:

- Bare bus wire that consists of a single strand of wire that is of sufficient cross-section to be compatible with the electrical requirements of the circuit without the use of sleeving or other insulation.
- Sleeved bus wire that consists of a single-strand of bare buswire (see above) that is covered by insulation tubing.
- Insulated bus wire that consists of a single-strand wire purchased with its own insulation, such as varnish coating.

- Insulated stranded wire that consists of multiple strands of wire purchased with an insulating material, such as a polymer coating.

8.2.11.3 Application The designer should ensure that the use of jumper wires **shall** adhere to the following rules:

- Bare bus wires should not be longer than 25 mm [0.984 in].
- Bare bus wires **shall** not cross over board conductors.
- Bend radii for jumper wires should conform to that of normal component bend requirements (see 8.1.11).
- The shortest X-Y path of jumper routing should be used unless board design considerations dictate otherwise.

Sleeving **shall** be of sufficient length to ensure that its slippage at either end of the jumper wire will not result in a gap between the insulation and solder connection or wire bend that violates minimum electrical clearance distances. Also, the sleeving chosen **shall** be able to withstand the jumper wire or printed board soldering operations.

8.2.12 Heat Shrinkable Devices Heat shrink soldering devices are typically used to terminate shields on cables. The devices are composed of a solder ring enclosed in a solder sleeve insulator. The device is placed over the terminations to be soldered and heated with a hot air device. The heat melts the solder to form a joint and simultaneously encases the connection in insulation. Heat shrinkable devices may be self-sealing and may encapsulate the entire solder connection.

Solder sleeves compose a unique category because they form a portion of the design, yet are not integral to the printed wiring board.

8.2.13 Bus Bar Bus bars are usually in the form of preformed components that are part of the printed board assembly and serve the function of providing most, if not all, of the power and ground distribution over the board surface. Their use is primarily to minimize the use of board circuitry for power and ground distribution and/or to provide a degree of power and ground distribution not cost-effectively provided by the printed board.

The number of conductor levels in the bus bar, the type and number of their terminals, the size and finish of their conductors, and the dielectric strength of their insulation depends on the application. However, these parameters should be clearly defined on the procurement document for these parts. Whenever possible, their interface with the printed board should be at plated-through holes, while conforming to conventional lead size-to-hole and lead bending requirements (see 8.1.11). Also, for optimum board design efficiency, the bus bar terminals should interface with the board on a uniform termination pattern, may share the same holes as an integrated circuit and may be placed under an integrated circuit.

8.2.14 Flexible Cable When the design includes flexible cable becoming part of a printed circuit board, the terminations **shall** be accomplished in a manner that imposes no undue stress on the cable/printed board interconnection.

Sometimes this interconnection uses pins, where a pin passes through the board and the flexible cable to provide the proper interconnection. At other times, the flexible cable may be surface soldered directly to land patterns on the printed board or may be integral to the printed board as in rigid-flex applications. Proper mechanical support, using tie-down bars, or adhesives, **shall** be used to prevent stresses on the solder joints.

8.3 Through-Hole Requirements For automatic assembly of boards with components whose leads pass through the board, specific consideration should be given to providing the allowable clearances for the insertion and clinching of leads of the components. See 8.3.1 through 8.3.1.5 and IPC-CM-770 for specific details.

8.3.1 Leads Mounted in Through-Holes Part attachment **shall** be described on the assembly drawing following the methods specified herein. Requirements for lead-to-hole relationships are detailed in 9.2.3 through 9.3 of the related design sectional. Component leads, jumper wires and other leads **shall** be mounted such that there is only one lead in any one hole except as specified in 8.2.13. The recommended design for component leads in unsupported holes **shall** be such that they extend a minimum of 0.50 mm [0.020 in] and a maximum of 1.5 mm [0.0591 in] from the surface of the plating or foil. Component leads in supported holes **shall**, as a minimum, be discernable in the completed solder connection. The lead should not extend more than 1.5 mm [0.0591 in] (measured vertically) from the printed board surface, and the lead must not violate minimum electrical spacing requirements.

8.3.1.1 Straight Through-Hole Mounted Leads The straight-through leads on connectors or other devices with tempered leads may extend from 0.25 mm [0.00984 in] to 2.0 mm [0.0787 in], provided there is no electrical or mechanical interference.

8.3.1.2 Unclinched Leads Unclinched leads, straight or partially bent for retention **shall** be soldered in component holes or eyelets in accordance with J-STD-001 as applicable (see IPC-CM-770).

8.3.1.3 Clinched Leads When maximum mechanical retention of a lead or terminal is required by design, the lead or terminal **shall** be clinched. Component holes may

be plated-through holes, unsupported holes, or eyeletted holes. Clinching requirements **shall** be defined on the assembly drawing. The lead end **shall** not extend beyond the edge of its land, or its electrically connected conductor pattern, if it violates the minimum spacing requirements. Partial clinching of leads for part retention **shall** be considered under the requirements of 8.3.1.4 (see Figure 8-19).

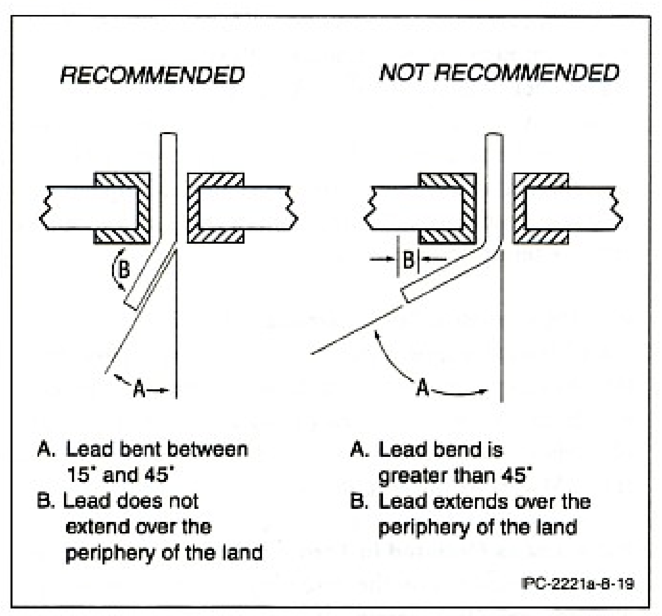


Figure 8-19 Partially Clinched Through-Hole Leads

Clinched leads are not applicable for tempered pins or for leads over 1.3 mm [0.0512 in] in diameter.

8.3.1.4 Partially Clinched Partially clinched leads are typically bent between 15° to 45° as measured from a vertical line perpendicular to the board. Partially clinched lead terminations **shall** not be used for manually inserted components except on diagonally opposite corner pins of dual in-line packages (DIPs) (see Figure 8-20).

8.3.1.5 Dual In-line Packages Leads on DIPs may be clinched in either direction for part retention. Clinch angle should be limited to 30° from the lead's original centerline. The clinch may be limted to two leads per side (four leads per part) (see Figure 8-20).

Dual in-line packages may be surface mounted provided the leads are intended for surface mount applications. For applications in which severe thermal stress is evident and the board provides the thermal management function, butt mounted packages **shall** not be used.

8.3.1.6 Axial Leaded Components The design for axial leaded components should follow 8.1.11. Lead bends **shall** be stress relieved as identified in that general paragraph. See Figure 8-2 for component body centering and Figure 8-9 for lead bend extensions.

The leads of components mounted horizontally with bodies in direct contact with the printed board **shall** be formed to ensure that excess solder is not present in the formed bends of the component leads (see Figure 8-21). Solder may be present in the formed bends of axial-leaded components provided that it is a result of normal lead interface wetting action and that the topside bend radius is discernible. Solder **shall** not extend so that it contacts the component body (see J-STD-001).

8.3.1.7 Radial-Lead Components

A. *Radial-Lead Components (2 Leads)* - Radial-leaded components vary in lead spacing. The design lead spacing is generally a function of the spacing at which the leads exit the body of the component (see Figure 8-22) and the nearest grid intersection.

Dual-lead components of configurations A through E of Figure 8-22 should be mounted freestanding with the larger sides perpendicular to the board surface within 15° as shown in Figure 8-23 when:

- Angularity is required for clearance in the next higher assembly; or

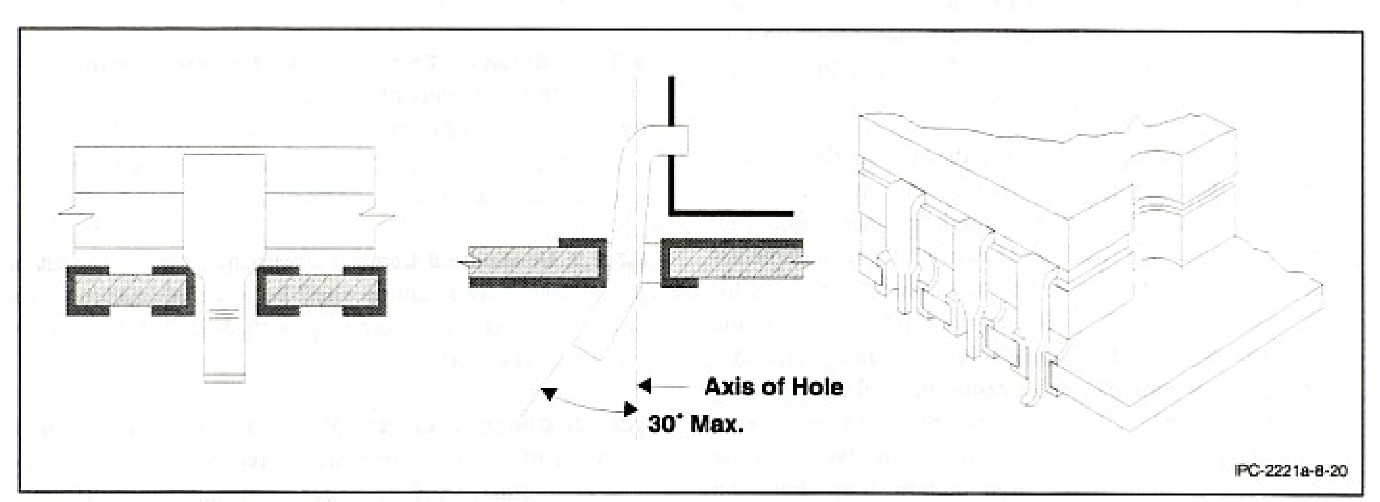


Figure 8-20 Dual In-Line Package (DIP) Lead Bends

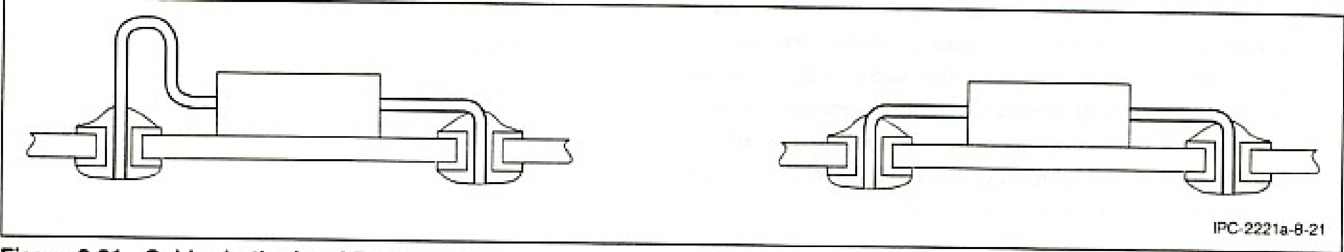


Figure 8-21 Solder in the Lead Bend Radius

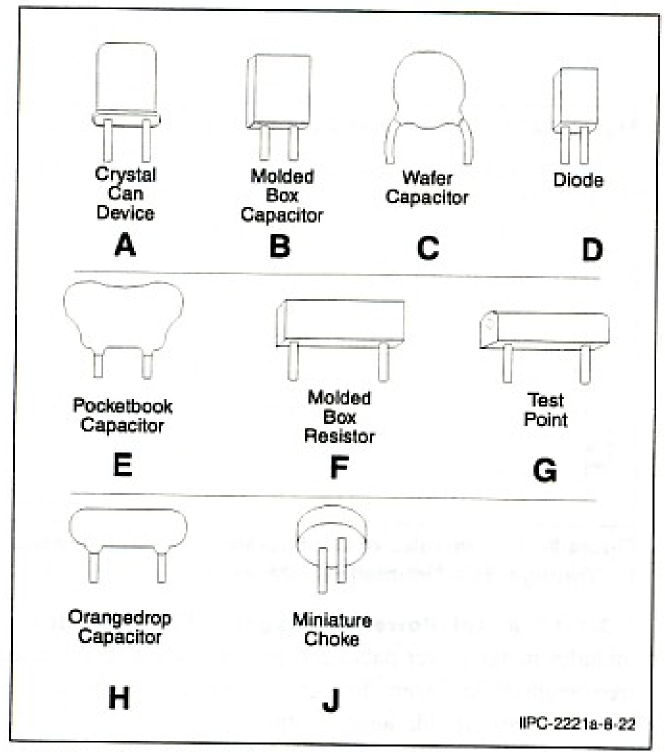


Figure 8-22 Two-Lead Radial-Leaded Components

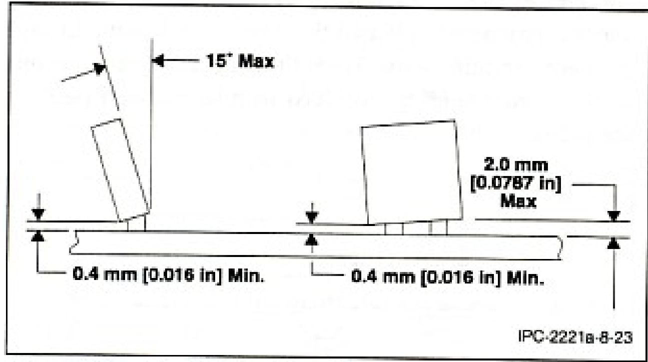


Figure 8-23 Radial Two-Lead Component Mounting, mm [in]

- That edge of the body nearest the surface of the board parallels the board surface within 10° and is no less than 1.0 mm [0.0394 in] and no more than 2.3 mm [0.0906 in] from the surface. Components of configurations F through J of Figure 8-22 are not included under the angularity exception.

Radial-leaded components with coating meniscus on one or more leads should be mounted such that there is visible clearance between the meniscus and the solder fillet. Trimming of the meniscus is prohibited (see Figure 8-24).

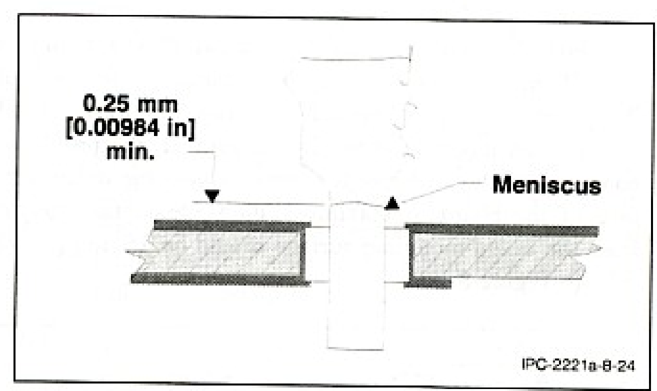


Figure 8-24 Meniscus Clearance, mm [in]

B. *Radial-Leaded Components (3 or more Leads)* - Radial-leaded components with three or more leads vary in lead spacing. The design lead spacing is generally a function of the spacing at which the leads exit from the body of the component (see Figure 8-25) and the nearest pattern of grid intersections that provides for suitable conductor routing.

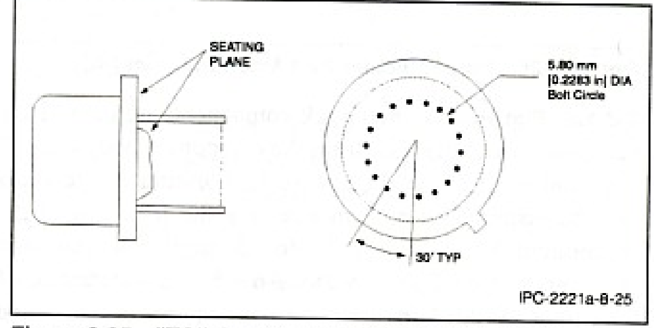


Figure 8-25 "TO" Can Radial-Leaded Component, mm [in]

C. *Class 3 High Reliability Requirements* - For Class 3 high reliability applications, components **shall** be mounted freestanding (i.e., with the base surface separated from the surface of the board with no support other than the component leads) only if the weight of

the component is 3.5 gm per lead or less. When components have an integral seating plane, the seating plane may be in contact with the board. When components are mounted freestanding, the spacing between the surface of the component and the surface of the board **shall** be a minimum of 0.25 mm [0.00984 in] and a maximum of 2.5 mm [0.0984 in].

In no instance **shall** nonparallelism result in nonconformance with the minimum or maximum spacing limit.

8.3.1.8 Perpendicular (Vertical) Mounting Axial-leaded components weighing less than 14 grams may be mounted on the assembly using vertical mounting criteria that have the major axis of the component body perpendicular to the board surface. The space between the end of the component body (or lead weld) and the board **shall** be a minimum of 0.25 mm [0.00984 in]. Height restriction for general component mounting normally pertains to axial-leaded components mounted vertically. In general, the profile of components should be kept as low as possible to the surface of the board. A maximum allowable vertical height from the board mounting surface should be 15 mm [0.591 in], see Figure 8-26.

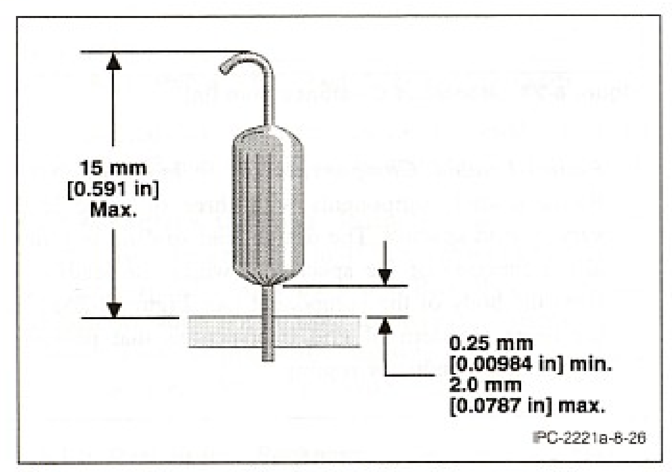


Figure 8-26 Perpendicular Part Mounting, mm [in]

8.3.1.9 Flat-Packs Flat-pack components normally have flat ribbon leads that exit from the component body on 1.27 mm lead centers (see Figure 8-27). Forming of the leads may be required to prevent stressing the lead exit at the component body, especially for through-hole mounted applications (see Figure 8-28). An off-board clearance of 0.25 mm [0.00984 in] minimum is required for cleaning purposes.

The body of the component **shall** not be in contact with any vias unless the vias are coated per 8.1.10. Leads **shall** extend from the body of the part a minimum of one lead diameter or thickness but not less than 0.8 mm [0.0315 in] from the body or weld before the start of the bend radius (see Figure 8-9 and J-STD-001).

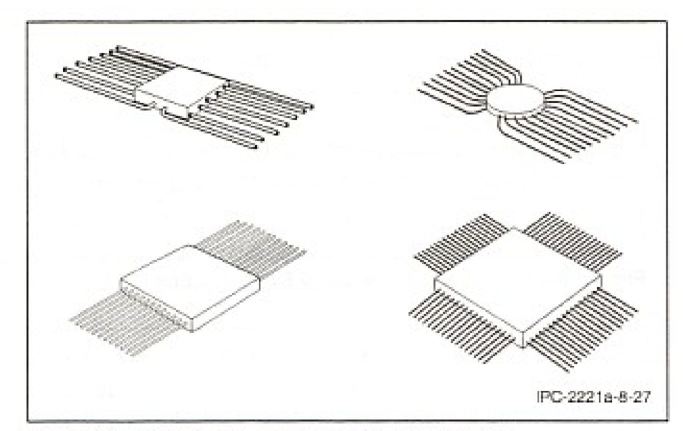


Figure 8-27 Flat-Packs and Quad Flat-Packs

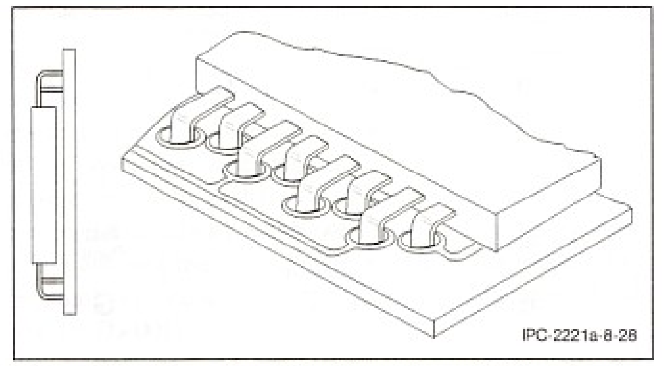


Figure 8-28 Examples of Configuration of Ribbon Leads for Through-Hole Mounted Flat-Packs

8.3.1.10 Metal Power Packages When the design includes metal power packages, they **shall** not be mounted free standing. Stiffeners, heatsinks, frames and spacers may be utilized to provide needed support.

Metal power packages with leads that are neither tempered nor greater than 1.25 mm [0.0492 in] (compliant leads) may be terminated in plated-through holes or with through-the-board terminations. With through-the-board terminations the leads **shall** be provided with stress relief (see Figure 8-29).

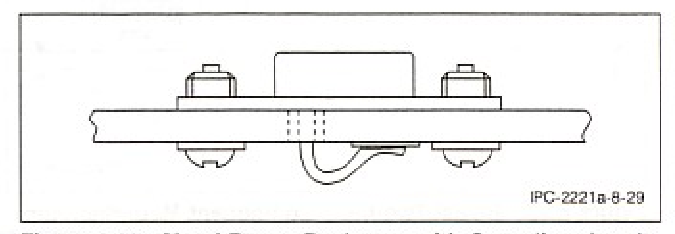


Figure 8-29 Metal Power Packages with Compliant Leads

With plated-through hole terminations the package **shall** be mounted off the board and spacers used to provide stress relief for the leads (see Figure 8-30). Side mounting may also be employed.

Metal power packages with noncompliant leads may also be mounted with the leads terminated in plated-through holes or with through hole termination. The requirements

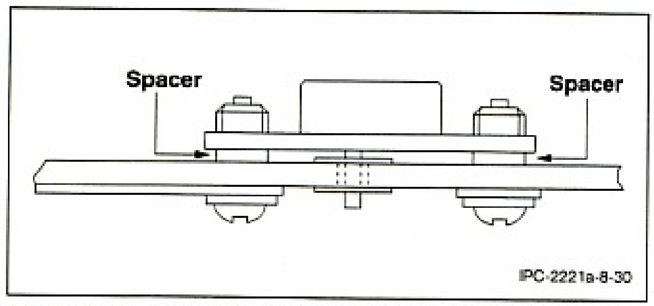


Figure 8-30 Metal Power Package with Resilient Spacers

for plated-through hole terminations **shall** be the same as those for packages with compliant leads (see Figure 8-29). For through-the-board terminations, the leads **shall** be terminated to the board by jumper connections (see Figure 8-31). The termination of the jumper to the board **shall** be made either to a plated-through hole or to a land.

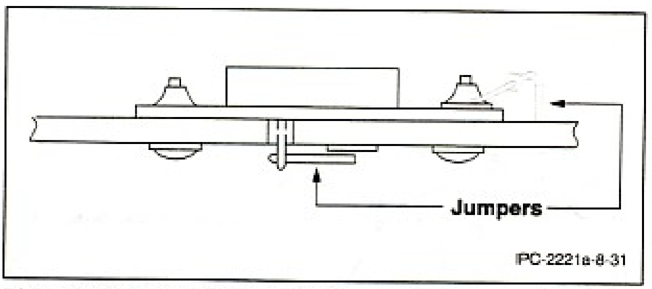


Figure 8-31 Metal Power Package with Noncompliant Leads

Care must be exercised when the mounting utilizes spacers to ensure that any electrical connection between the component case and the board circuitry remains constant under all operating conditions.

Whenever the terminations are made in plated-through holes, the mounting **shall** ensure that the connections can be cleaned between the component and the board. Metal power packages, the standoffs, heatsink frames, and resilient spacers on which metal power packages are mounted **shall** be of configurations which do not block plated through-holes, preclude excessive stresses (provide stress relief), and facilitate cleaning.

8.4 Standard Surface Mount Requirements Automatic assembly considerations for surface mounted components are driven by pick-and-place machines used to place/position chip components, discrete chip carriers, small outline packages, and flat packs. Printed board designs **shall** maintain appropriate clearances for the automatic pick-and-place equipment to position the parts in their proper orientation and allow sufficient clearances for the placement heads (see IPC-SM-780).

Typically, fine pitch devices could be between 250 and 775 mm^2 case size for automatic placement without vision. Generally, the largest component that can be placed with vision alignment is 1300 mm^2 [51.181 in^2], measured to the outside of the leads. Large packages exaggerate the effects of the thermal mismatch between the component and substrate. Normally, the minimum size leadless component that can be placed with automatic equipment is 1.5 mm [0.0591 in] nominal length by 0.75 mm [0.0295 in] nominal width. Smaller components require high placement accuracy. Vacuum pickup with standard equipment is also difficult.

Avoid extremely small passive components. Leadless passive components should have an aspect ratio greater than one and less than three. High aspect ratio parts tend to fracture during soldering. Square devices (aspect ratio = 1) are difficult to orient.

Smaller components are easier to solder, but footprints must be large enough to permit reliable placement of adhesive without smearing onto the conductor. Avoid components which require mounting land spacings (on the same component) closer than 0.75 mm [0.0295 in], due to process limitations on applying (chip bonding or thermal adhesive). High profile SMT components (higher than 2.5 mm [0.0984 in]) interfere with wave solder flow to adjacent components, and should be avoided.

Special orientation symbols should be incorporated into the design to allow for ease of inspection of the assembled surface mounted part. Techniques may include special symbols, or special land configurations to identify such characteristics as pin 1 of an integrated circuit package.

8.4.1 Surface-Mounted Leaded Components The requirements and considerations of 8.1.7 apply to the surface-mounting of leaded components. Lead forming is a major design consideration. Custom lead forms should be described on the assembly drawing to provide for lead stress relief to ensure fit to the land pattern to allow under-body clearance for cleaning, and to provide any designed-in provisions for thermal transfer (see Figure 8-32 and IPC-SM-782).

Axial leaded components may be surface mounted provided the leads are coined (see Figure 8-33). However, they may never be surface mounted in a perpendicular orientation (see Figure 8-26).

8.4.2 Flat-Pack Components Flat-pack components normally have flat ribbon leads that exit from the component body on 1.27 mm [0.05 in] lead centers (see Figure 8-34). Although they generally have from 14 to 16 leads, flat-packs with up to 50 leads are available.

When planar mounted flat-packs require lead forming, the leads **shall** be configured as shown in Figure 8-34. Non-insulated parts mounted over exposed circuitry **shall** have their leads formed to provide a minimum of 0.25 mm [0.00984 in] between the bottom of the component body

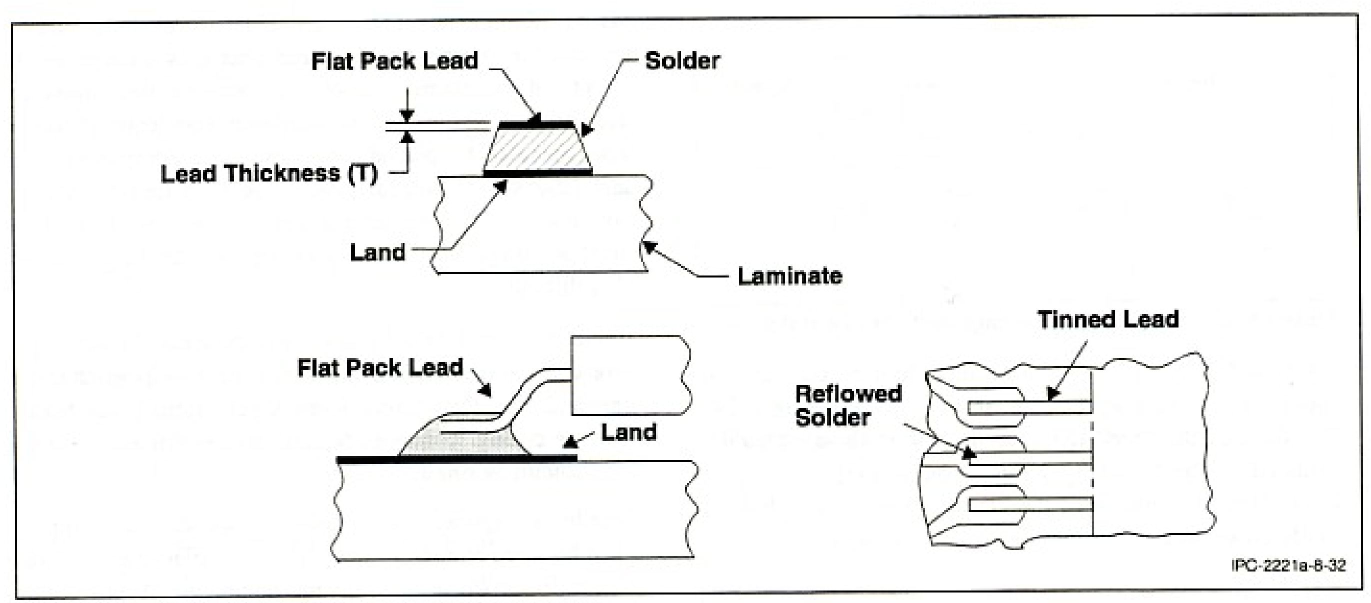


Figure 8-32 Examples of Flat-Pack Surface Mounting

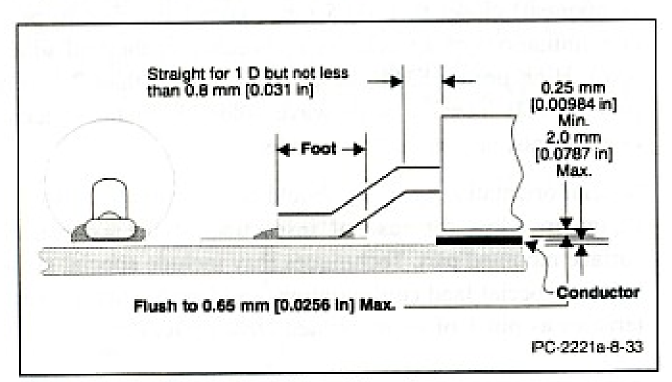


Figure 8-33 Round or Coined Lead

and the exposed circuitry. The maximum clearance between the bottom of the leaded component body and the printed wiring surface should be 2.0 mm [0.0787 in]. Parts insulated from circuitry or over surfaces without exposed circuitry may be mounted flush. If the component requires thermal transfer to the board, special consideration for cleaning should be given.

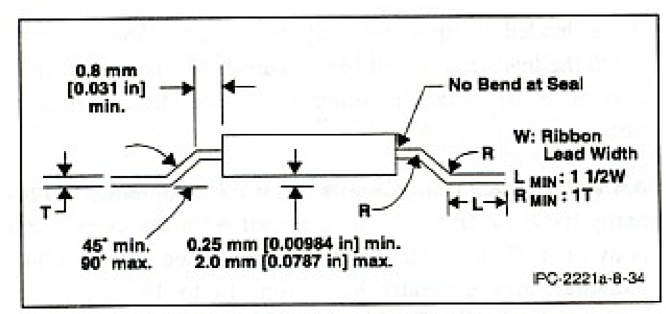


Figure 8-34 Configuration of Ribbon Leads for Planar Mounted Flat-Packs

8.4.3 Ribbon Lead Termination Flat-wire ribbon leads may be attached to lands on the printed board (see Figure 8-35). Connections **shall** be made by soldering or wire bonding only.

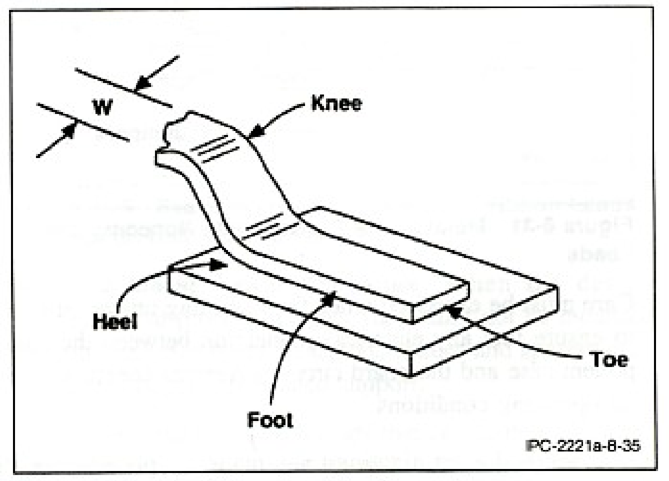


Figure 8-35 Heel Mounting Requirements

8.4.4 Round Lead Termination In some instances, components with round leads may be attached to the surface lands without first passing through a hole. The land **shall** be designed with the proper shape and spacing to comply with proper soldering techniques. Components with axial leads of round cross-section may be coined or flattened to provide positive mounting (see Figure 8-33).

8.4.5 Component Lead Sockets Component lead sockets may be allowed for Class 3 high reliability requirements when engineering analysis proves acceptable. Care should be taken in specifying the use of nonnoble platings or finishes on either sockets or the component leads because of the possibility of producing inherent heat or open circuits due to fret corrosion during vibration or temperature cycling.

8.5 Fine Pitch SMT (Peripherals) See SMC-TR-001.

8.6 Bare Die

8.6.1 Wire Bond See IPC-MC-790.

8.6.2 Flip Chip See J-STD-012.

8.6.3 Chip Scale Chip scale packaging is, by definition, a package in which the area is no greater than 120% of the area of the die. Placement is frequently the rate limiting step, and the most expensive in the assembly process. The factors that contribute most significantly to the cost include:

- Throughput (number of placements/time).
- Vision system requirements.
- Die presentation options.
- Chip to substrate alignment accuracy.
- Chip to substrate coplanarity requirements.
- Additional required features such as supplying heat and pressure during assembly.

For further discussion of chip scale packaging and placement, see J-STD-012.

8.7 Tape Automated Bonding See SMC-TR-001.

8.8 Solderball (BGA, mBGA, etc.) See J-STD-013 and IPC-7095.

9 HOLES/INTERCONNECTIONS

9.1 General Requirements for Lands with Holes Lands **shall** be provided for each point of attachment of a part lead or other electrical connection to the printed board. Circular lands are most common, but it should be noted that other land shapes may be used to improve producibility. If breakout is allowed, modified land shapes **shall** be used. These may include, for example, filleting to create additional land area at the conductor junction, corner entry on rectangular lands or "keyholing" to create additional land area along the axis of the incoming lead (see Figure 9-1). The modified land shape **shall** provide for the current carrying capacity of the circuit design.

9.1.1 Land Requirements All lands and annular rings **shall** be maximized wherever feasible, consistent with good design practice and electrical clearance requirements. To meet the annular ring requirements specified in section 9.1.2, the minimum land surrounding a supported, or unsupported, hole **shall** be determined by the following.The worst-case land-to-hole relationship is established by the equation:

Land size, minimum = a + 2b + c

where:

a = Maximum diameter of the finished hole.
Note: For external layers, the requirement is the maximum diameter of the finished hole. For internal layers, the drill hole diameter is used.

b = Minimum annular ring requirements (see Section 9.1.2).
Note: Etchback must be included within the calculation.*

c = A standard fabrication allowance, detailed in Table 9-1, which considers production master tooling and process variations required to fabricate boards.
Note: Refer to the specific sectional design standard for additional processing allowance.

*Etchback, when required will reduce the insulation area that supports the internal land. The minimum annular ring considered in the design **shall** not be less than the maximum etchback allowed.

9.1.2 Annular Ring Requirements An annular ring **shall** be required for all plated-through holes in Class 3 designs. The performance specifications for Class 1 and Class 2 products may allow partial hole breakouts. The design for these products should take into consideration that breakout is undesirable and the design should require adequate hole and land size so that breakout does not appear in the finished product. Landless holes or holes with partial circumscribing lands **shall** only be used when approved by the acquiring activity prior to the start of the design process and require conformance specimen that reflect the approach being used.

The minimum annular ring on external layers is the minimum amount of copper (at the narrowest point) between the edge of the hole and the edge of the land after plating of the finished hole (see Figure 9-2). The minimum annular ring on internal layers is the minimum amount of copper (at the narrowest point) between the edge of the drilled hole and the edge of the land after drilling the hole (see Figure 9-3).

A. *External Annular Ring*—The minimum annular ring for unsupported and supported holes **shall** be in accordance with Table 9-2 and Figure 9-2.

B. *Internal Annular Ring*—The minimum annular ring for internal lands on multilayer and metal core boards **shall** be in accordance with Table 9-2 and Figure 9-3. Etchback, when required, will reduce the insulation supporting the annular ring of internal lands. The minimum annular ring considered in the design **shall** be not less than the maximum etchback allowed.

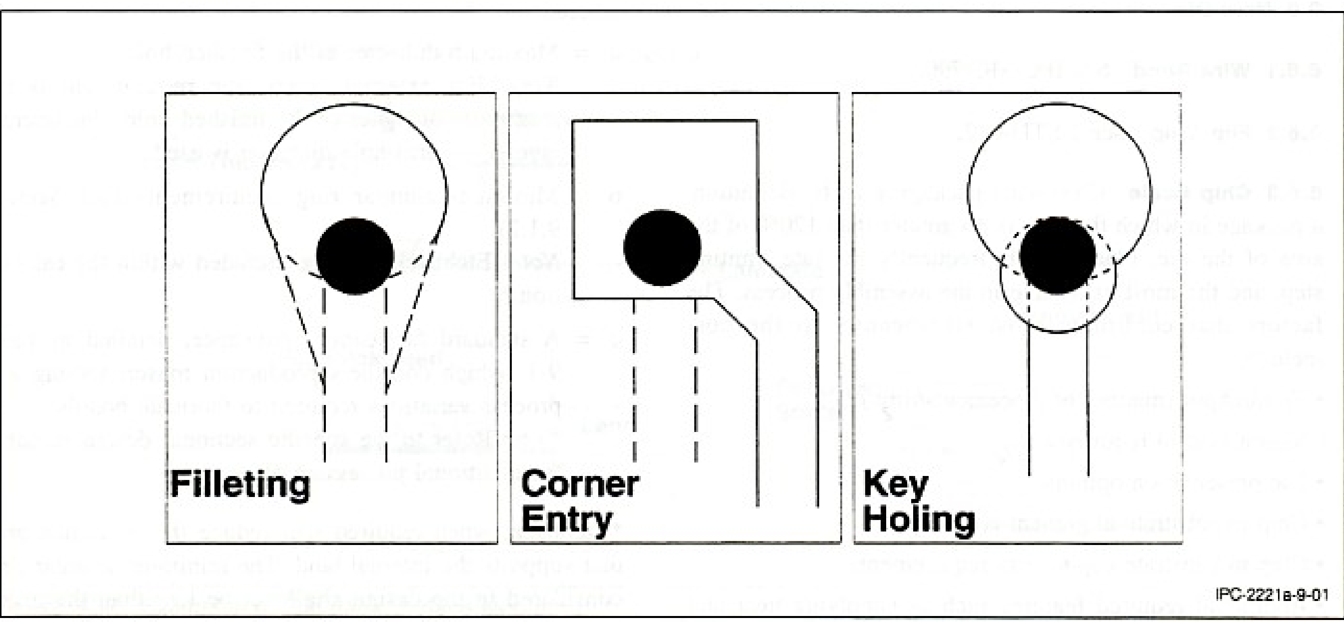


Figure 9-1 Examples of Modified Land Shapes

Table 9-1 Minimum Standard Fabrication Allowance for Interconnection Lands

Level A	Level B	Level C
0.4 mm [0.016 in]	0.25 mm [0.00984 in]	0.2 mm [0.0079 in]

1. For copper weights greater than 1oz/sq.ft., add 0.05 mm [0.0197 in] minimum to the fabrication allowance for each additional oz/sq. ft. of copper used.
2. For more than 8 layers add 0.05 mm [0.0197 in].
3. See 1.6.3 for definition of Levels A, B and C.

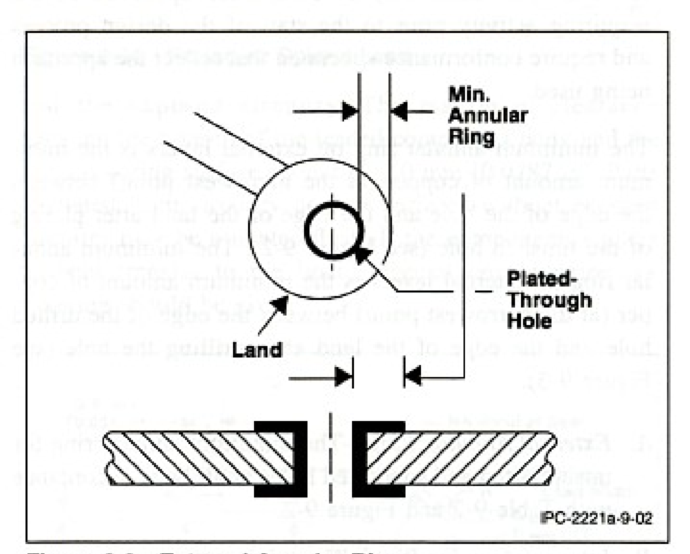


Figure 9-2 External Annular Ring

9.1.3 Thermal Relief in Conductor Planes Thermal relief is only required for holes that are subject to soldering in large conductor areas (ground planes, voltage planes, thermal planes, etc.). Relief is required to reduce soldering dwell time by providing thermal resistance during the soldering process.

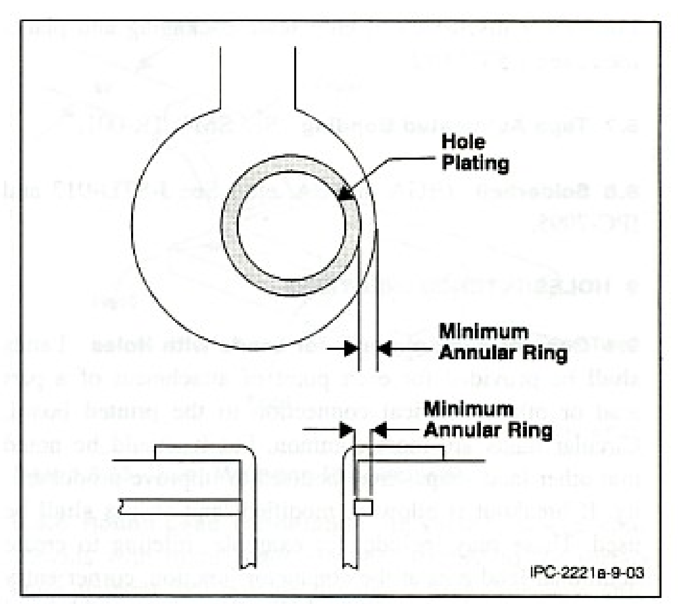


Figure 9-3 Internal Annular Ring

Table 9-2 Annular Rings (Minimum)

Annular Ring	Class 1, 2, and 3
Internal Supported	0.025 mm [0.00098 in]
External Supported	0.050 mm [0.00197 in]
External Unsupported	0.150 mm [0.005906 in]

These type connections **shall** be relieved in a manner similar to that shown in Figure 9-4. The relationship between the hole size, land and web area is critical. See the sectional standards for more detailed information.

9.1.4 Lands for Flattened Round Leads Flattened round (coined) leads **shall** have a land which will provide the

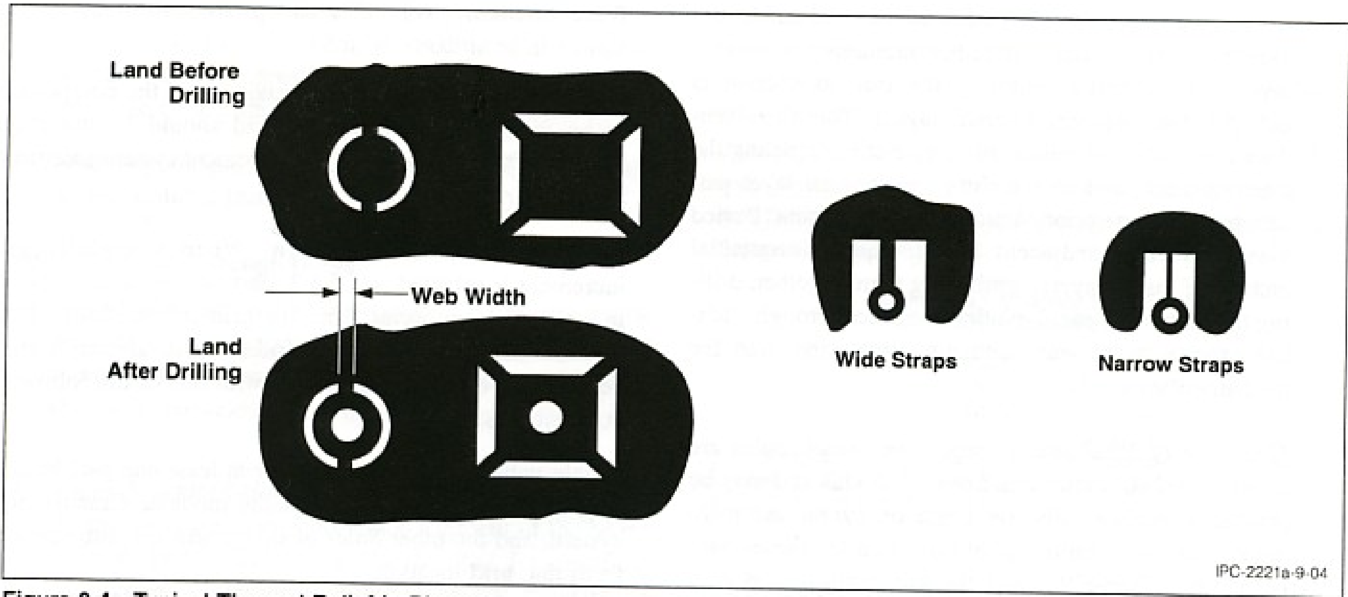


Figure 9-4 Typical Thermal Relief in Planes

seating so that the heel and the terminal relationship is in accordance with Figure 8-33.

Lead and land size should be designed to minimize side overhang. (Class 3 product allows up to 1/4 of the lead diameter to overhang.) Toe overhang is acceptable provided it does not violate the minimum designed conductor spacing. If flattened leads are used, the flattened thickness **shall** not be less than 40% of the original diameter (see J-STD-001).

9.2 Holes

9.2.1 Unsupported Holes These types of holes pass through the entire board thickness. They do not contain plating or other types of reinforcement. They may be used for tooling, mounting or component attachment.

9.2.1.1 Tooling Holes This type of hole is a physical feature in the form of a hole, or slot, on a printed board fabrication panel or assembly panel. Tooling features are used exclusively to position a printed board or assembly during fabrication, assembly, and test procedures. This includes:

a) Registration of phototooling.
b) Positioning core layers during lamination.
c) Panels during drilling.
d) Boards at bare board testing.
e) Panels of boards during automated assembly.
f) Functional test.

The designer is responsible for indicating the tooling holes that stay with the board or panel. The board manufacturer is responsible for determining the tooling holes needed for board fabrication.

9.2.1.2 Mounting Holes These are holes that are used for the mechanical support of a printed board or for the mechanical attachment of components to a printed board.

9.2.2 Plated-Through Holes This type of hole has plating on its wall that makes an electrical connection between conductive patterns on internal or external layers, or both, of a printed board.

These holes may also be used for component attachment, mounting, electrical interconnection or thermal transfer.

9.2.2.1 Blind and Buried Vias Plated-through holes connecting two or more conductive layers of multilayer printed board, but not extending fully through all layers of the base material comprising the board, are called blind and buried vias.

A) *Blind Vias* Blind via plated-through holes extend from the surface and connect the surface layer with one or more internal layers.. The blind via can be produced by two methods: (1) After multilayer lamination by drilling a hole from the surface to the internal layers desired and electrically interconnecting them by plating the blind via holes during the plating process; or (2) Before multilayer lamination by drilling the blind via holes from the surface layers to the first or last buried layers and plating them through, imaging and etching the internal sides, and then laminating them in the multilayer bonding process. For the second process if an interconnection is desired between the surface layer and more than one internal layer, sequential etching, laminating, drilling and plating-through of these layers together before final multilayer lamination is required. Blind via holes should be filled or plugged with a polymer or solder resist to prevent solder from entering them as solder in the small holes decreases reliability.

B) *Buried Vias* Buried via plated-through holes do not extend to the surface but rather interconnect internal layers only. Most commonly the interconnection is between two adjacent internal layers. These are produced by drilling the thin laminate material, plating the holes through, and then etching the internal layer pattern on the layers prior to multilayer lamination. Buried vias between nonadjacent layers requires sequential etching of inside layers, laminating them together, drilling the laminated panel, plating the holes through, etching external sides and laminating this panel into the final multilayer panel.

C) *Hole Size of Blind and Buried Vias* Small holes are usually used for either blind or buried vias and may be produced mechanically, by laser, or by plasma techniques. The minimum drilled hole size for buried vias is shown in Table 9-3 and the minimum drilled hole size for blind vias is shown in Table 9-4. In either case plating aspect ratios must be considered as small, deep blind vias are very difficult to plate due to decreased throwing-power and limited plating solution exchange in the holes. Blind and buried vias may be plated shut; thus, the master drawing call out should be similar to that used for through-hole vias. See sectional standards for more information.

Table 9-3 Minimum Drilled Hole Size for Buried Vias

Layer Thickness	Class 1	Class 2	Class 3
<0.25 mm [<0.00984 in]	0.10 mm [0.00393 in]	0.10 mm [0.00393 in]	0.15 mm [0.00591 in]
0.25 - 0.5 mm [0.020 in]	0.15 mm [0.00591 in]	0.15 mm [0.00591 in]	0.20 mm [0.00787 in]
0.5 mm [0.020 in]	0.15 mm [0.00591 in]	0.20 mm [0.00787 in]	0.25 mm [0.00984 in]

Table 9-4 Minimum Drilled Hole Size for Blind Vias

Layer Thickness	Class 1	Class 2	Class 3
<0.10 mm [<0.00393 in]	0.10 mm [0.00393 in]	0.10 mm [0.00393 in]	0.2 mm [0.0079 in]
0.10 - 0.25 mm [0.00984 in]	0.15 mm [0.00591 in]	0.20 mm [0.00787 in]	0.3 mm [0.012 in]
0.25 mm [0.00984 in]	0.20 mm [0.00787 in]	0.30 mm [0.0118 in]	0.4 mm [0.016 in]

9.2.2.2 Thermal Vias Thermal vias are plated-through holes usually located under high power devices in groups that form a connection to the device package, either directly or through a thermally conductive medium. Their connection to internal planes and/or external planes serves to transfer heat out of the device packages. Thermal vias are typically larger than blind and buried vias and are not subjected to the same integrity requirements as other component and via holes.

9.2.3 Location All holes and profiles **shall** be dimensioned in accordance with 5.4.

Note: The lead patterns of the majority of the components to be mounted on a printed board should be the major influence in the choice of a measurement system (metric or imperial).

9.2.4 Hole Pattern Variation When a modular grid increment is selected, see 5.4.2, parts whose leads emanate in a pattern that varies from the grid intersections of the modular dimensioning system of the printed board, **shall** be mounted on the printed board with one of the following hole patterns:

A hole pattern where the hole, for at least one part lead, is located at a grid intersection of the modular dimensioning system, and the other holes of the pattern are dimensioned from that grid location.

A hole pattern where the center of the pattern is located at a grid intersection of the modular dimensioning system, and all holes of the pattern are dimensioned from that grid location.

9.2.5 Tolerances

9.2.5.1 Hole Location Tolerances Table 9-5, based on glass/epoxy materials, shows the values for hole location tolerances that are to be applied to the basic hole position. All tolerances are expressed as diameter about true position. These tolerances only take into account drill positioning and drill drift. The basic hole position may be further affected by material thickness, type and the copper density. The effect is usually a reduction (shrinkage) between basic hole positions.

Table 9-5 Minimum Hole Location Tolerance, dtp

Level A	Level B	Level C
0.25 mm [0.00984 in]	0.2 mm [0.0079 in]	0.15 mm [0.00591 in]

9.2.5.2 Unsupported Holes

A) *Tooling Holes* Tooling holes are toleranced tightly in order to avoid movement between the tooling pin and the board. This is especially important if the holes are being used for registration. Registration pins are usually very precise, with tolerances in the range of 0.025 mm [0.001 in] or less. The holes also have precise tolerances which are generally in the range of 0.05 mm [0.002 in]. Maximum Material Condition (MMC) and Least Material Condition (LMC) are terms used to describe the relationship between the hole and the pin.

Line to line conditions are considered as an interference fit, thus the MMC of the hole (when the hole is smallest) is usually considered with as small a clearance as

possible with the MMC of the pin (when the pin is as large as possible). A 0.025 mm [0.001 in] clearance is usually sufficient provided that the hole does not get too large or the pin too small.

B) Mounting Holes Tolerances normally follow standard fit and fastener techniques (see IPC-2615).

9.2.5.3 Plated-Through Holes

A) Plated-Through Hole Tolerances When using the basic dimensioning system, plated-through holes used to attach component leads or pins to the printed board should be expressed in terms of MMC and LMC limits.

B) Board Mounting Holes These are holes that are used for the mechanical support and attachment of the board to its assembly. They may also be used for electrical connections. Tolerances normally follow standard fit and fastener techniques (see IPC-2615).

9.2.6 Quantity A separate component hole **shall** be provided for each lead, terminal of a part, or end of a jumper wire that is to be through-hole mounted, except as specified in 8.2.11.

9.2.7 Spacing of Adjacent Holes The spacing of unsupported or plated-through holes (or both) **shall** be such that the lands surrounding the holes meet the spacing requirements of 6.3. Consideration should be given to the printed board material structural requirements, with the residual laminate material being no less than 0.5 mm [0.020 in].

9.2.8 Aspect Ratio The aspect ratio of plated-through holes plays an important part in the ability of the manufacturer to provide sufficient plating within the plated-through hole.

10 GENERAL CIRCUIT FEATURE REQUIREMENTS

10.1 Conductor Characteristics Conductors on the printed board may take a variety of shapes. They may be in the form of single conductor traces, or conductor planes.

Critical pattern features which may affect circuit performance such as distributed inductance, capacitance, etc., **shall** be identified, unless the procurement contract requires the delivery of a stable master produced within the tolerance required for circuit performance.

10.1.1 Conductor Width and Thickness The width and thickness of conductors on the finished printed board **shall** be determined on the basis of the signal characteristics, current carrying capacity required and the maximum allowable temperature rise. These **shall** be determined using Figure 6-4. In determining the thickness of conductors on the finished printed board, the designer should take into consideration that processing may vary the thickness of copper on circuit layers. Circuits sensitive to voltage drop should take this into account and consider stating a minimum thickness value based on design constraints. Tables 10-1 and 10-2 are intended to provide guidance between design and fabrication facilities and are not to be interpreted as a design requirement.

Table 10-1 Internal Layer Foil Thickness After Processing

Weight, oz. [µm]	Absolute Cu Min. (IPC-4562 less 10% reduction) (µm) [µin]	Maximum Variable Processing Allowance Reduction*	Minimum Final Finish after Processing (µm) [µin]
1/8 oz. [5.10]	4.60 [181]	1.50	3.1 [122]
1/4 oz. [8.50]	7.70 [303]	1.50	6.2 [244]
3/8 oz. [12.00]	10.80 [425]	1.50	9.3 [366]
1/2 oz. [17.10]	15.40 [606]	4.00	11.4 [449]
1 oz. [34.30]	30.90 [1,217]	6.00	24.9 [980]
2 oz. [68.60]	61.70 [2,429]	6.00	55.7 [2,193]
3 oz. [102.90]	92.60 [3,646]	6.00	86.6 [3,409]
4 oz. [137.20]	123.50 [4,862]	6.00	117.5 [4,626]
Above 4 oz. [137.20]		6.00	4 µm [157 µin] below min. thickness listed for that foil thickness in IPC-4562

* Process allowance reduction does not allow for rework processes for weights below ½ oz. For ½ oz. and above, the process allowance reduction allows for one rework process.

When product safety certification organizations such as Underwriters Laboratories (UL) impose requirements, the specified minimum conductor width **shall** be within the limits approved by the safety certification organization for the printed board manufacturer. For ease of manufacturing and durability in usage, conductor width and spacing requirements should be maximized while maintaining the minimum desired spacing requirements. The nominal finished conductor width and acceptable tolerances, **shall** be shown on the master drawing.

When bilateral tolerances are required on the conductor, the nominal finished conductor width and the tolerances shown in Table 10-3, which are typical for 0.046 mm [0.00181 in] copper, **shall** be shown on the master drawing. This dimension need only be shown on the master drawing for a typical conductor of that nominal width.

If the tolerances in Table 10-3 are too broad, tighter tolerances than Table 10-3 can be agreed to between the user and supplier and **shall** be stated on the master drawing and considered Level C. Table 10-3 values are bilateral tolerances for finished conductors.

Table 10-2 External Conductor Thickness After Plating

Weight, oz. [µm]	Absolute Cu Min. (IPC-4562 less 10% reduction) (µm) [µin]	Plus minimum plating for Class 1 and 2 (20 µm)	Plus minimum plating for Class 3 (25 µm)	Maximum Variable Processing Allowance Reduction*	Minimum Surface Conductor Thickness after Processing (µm) [µin]	
					Class 1 & 2	Class 3
1/8 oz. [5.10]	4.60 [181]	24.60	29.60	1.50	23.1 [909]	28.1 [1,106]
1/4 oz. [8.50]	7.70 [303]	27.70	32.70	1.50	26.2 [1,031]	31.2 [1,228]
3/8 oz. [12.00]	10.80 [425]	30.80	35.80	1.50	29.3 [1,154]	34.3 [1,350]
1/2 oz. [17.10]	15.40 [606]	35.40	40.40	2.00	33.4 [1,315]	38.4 [1,512]
1 oz. [34.30]	30.90 [1,217]	50.90	55.90	3.00	47.9 [1,886]	52.9 [2,083]
2 oz. [68.60]	61.70 [2,429]	81.70	86.70	3.00	78.7 [3,098]	83.7 [3,295]
3 oz. [102.90]	92.60 [3,646]	112.60	117.60	3.00	109.6 [4,315]	114.6 [4,512]
4 oz. [137.20]	123.50 [4,862]	143.50	148.50	4.00	139.5 [5,492]	144.5 [5,689]

* Process allowance reduction does not allow for rework processes for weights below ½ oz. For ½ oz. and above, the process allowance reduction allows for one rework process.
Reference: Min. Cu Plating Thickness
Class 1 = 20 µm [787 µin]
Class 2 = 20 µm [787 µin]
Class 3 = 25 µm [984 µin]

Table 10-3 Conductor Width Tolerances for 0.046 mm [0.00181 in] Copper

Feature	Level A	Level B	Level C
Without plating	±0.06 mm [0.00236 in]	±0.04 mm [0.00157 in]	±0.015 mm [0.0005906 in]
With plating	±0.10 mm [0.00393 in]	±0.08 mm [0.00314 in]	±0.05 mm [0.0197 in]

The width of the conductor should be as uniform as possible over its length; however, it may be necessary because of design restraints to "neck down" a conductor to allow it to be routed between restricted areas, e.g., between two plated-through holes. The use of "necking down" such as that shown in Figure 10-1, can also be viewed as "beefing up." Single width, having a thin conductor throughout the board, as opposed to the thin/thick approach is less desirable from a manufacturing point of view as the larger width conductor is less rejectable due to edge defects rated as a percentage of the total width.

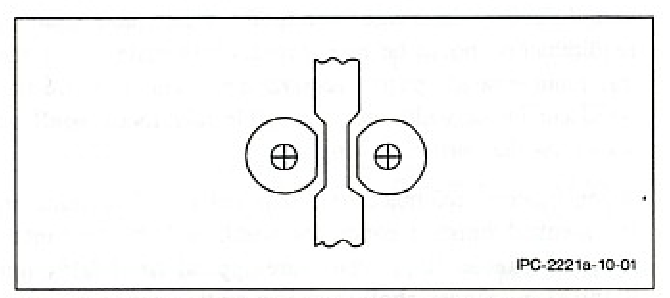


Figure 10-1 Example of Conductor Beef-Up or Neck-Down

In any event, if the conductor width change is used, the basic design requirements defined herein **shall** not be violated at the necking down location.

10.1.2 Electrical Clearance Clearances are applicable for all levels of design complexity (A, B, C) and performance classes (1, 2, 3). Conductive markings may touch a conductor on one side, but minimum spacing between the character marking and adjacent conductors **shall** be maintained (see Table 6-1).

To maintain the conductor spacing shown on the master drawing, space widths on the production master may require compensation for process allowances as defined in 10.1.1. Plated-through holes passing through internal foil planes (ground and voltage) and thermal planes **shall** meet the same minimum clearance between the plated-through hole and foil or ground planes as required for spacing between internal conductors (see 10.1.4). See 6.3 for more information on electrical clearance.

10.1.3 Conductor Routing The length of a conductor between any two lands should be held to a minimum. However, conductors which are straight lines and run in X, Y, or 45° directions are preferred to aid computerized documentation for mechanized or automated layouts. All conductors that change direction, where the included angle is less than 90°, should have their internal and external corners rounded or chamfered.

In certain high speed applications, specific routing rules may apply. A typical example is serial routing between signal source, loads and terminators. Routing branches (stubs) may also have specified criteria.

10.1.4 Conductor Spacing Minimum spacing between conductors, between conductive patterns, and between conductive materials (such as conductive markings, see 10.1.2, or mounting hardware) and conductors **shall** be defined on the master drawing. Spacings between conductors should be maximized and optimized whenever possible (see Figure 10-2). To maintain the conductor spacing shown on the

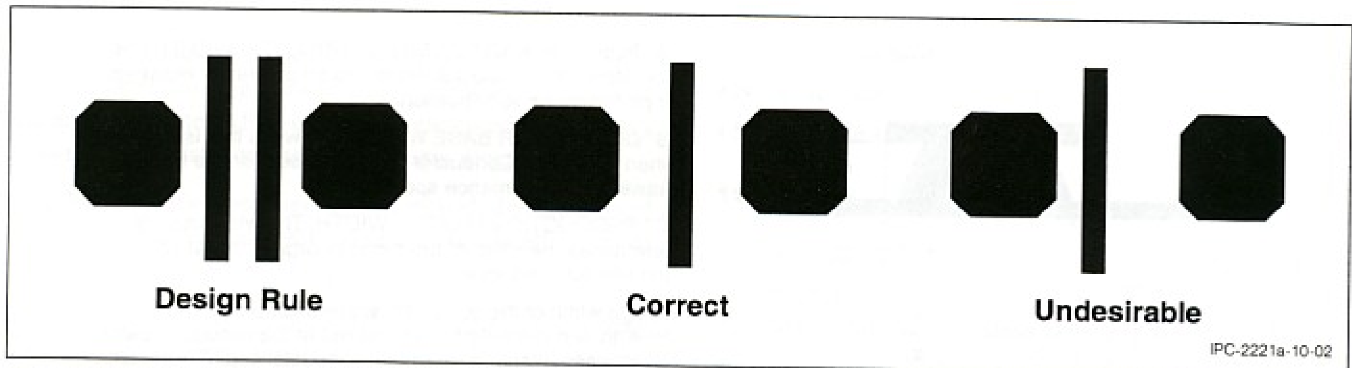


Figure 10-2 Conductor Optimization Between Lands

master drawing, conductor widths and spaces on the production master should be compensated for process allowances. These process allowances include but are not limited to, etch factors, conductor imperfections, and copper wicking between plated-through holes and adjacent plane layers.

10.1.5 Plating Thieves Plating thieves are added metallic areas which are nonfunctional. When located within the finished board profile, they allow uniform plating density, giving uniform plating thickness over the board surface. They **shall** neither adversely impact the minimum conductor spacing nor violate the required electrical parameters.

10.2 Land Characteristics

10.2.1 Manufacturing Allowances The design of all land patterns **shall** consider the manufacturing allowances, specifically those relating to conductor width and spacing.

Processing allowances similar to the characteristics shown in Figure 10-3 **shall** be built into the design to allow the manufacturer to produce a part that will meet the end-item requirements detailed on the master drawing (see IPC-D-310, and IPC-D-325).

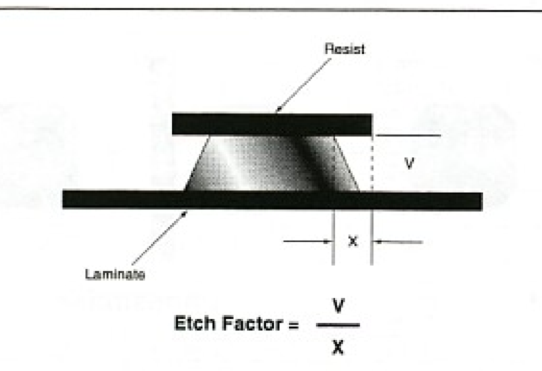
10.2.2 Lands for Surface Mounting When surface attachment is required, the requirements of 10.1 **shall** be considered in the design of the printed board. The selection of the design and positioning of the land geometry, in relation to the part, may significantly impact the solder joint. The possibility of heat thieving is reduced by "necking down" the conductor near the soldering area. The designer must understand the capabilities and limitations of the manufacturing and assembly operations (see IPC-SM-782).

The various soldering processes associated with surface mounting have specific land pattern requirements. It is desirable that the land pattern design be transparent to the soldering process to be used in manufacturing. This will be less confusing for the designer and reduce the number of land sizes.

10.2.3 Test Points When required by the design, test points for probing **shall** be provided as part of the conductor pattern, and **shall** be identified on the assembly drawing. Vias, wide conductors, or component mounting lands may be considered as probe points, provided that sufficient area is available for probing, and maintaining the integrity of the via, conductor, or component solder connection. Test points **shall** be free of coating material. After test has been completed, test points may be coated.

10.2.4 Orientation Symbols Special orientation symbols should be incorporated into the design to allow for ease of inspection of the assembled part. Techniques may include special symbols, or special land configurations to identify such characteristics as pin 1 of an integrated circuit package. Care should be taken to avoid adversely affecting the soldering process.

10.3 Large Conductive Areas Large conductive areas are related to specific products and are addressed in sectional design standards.



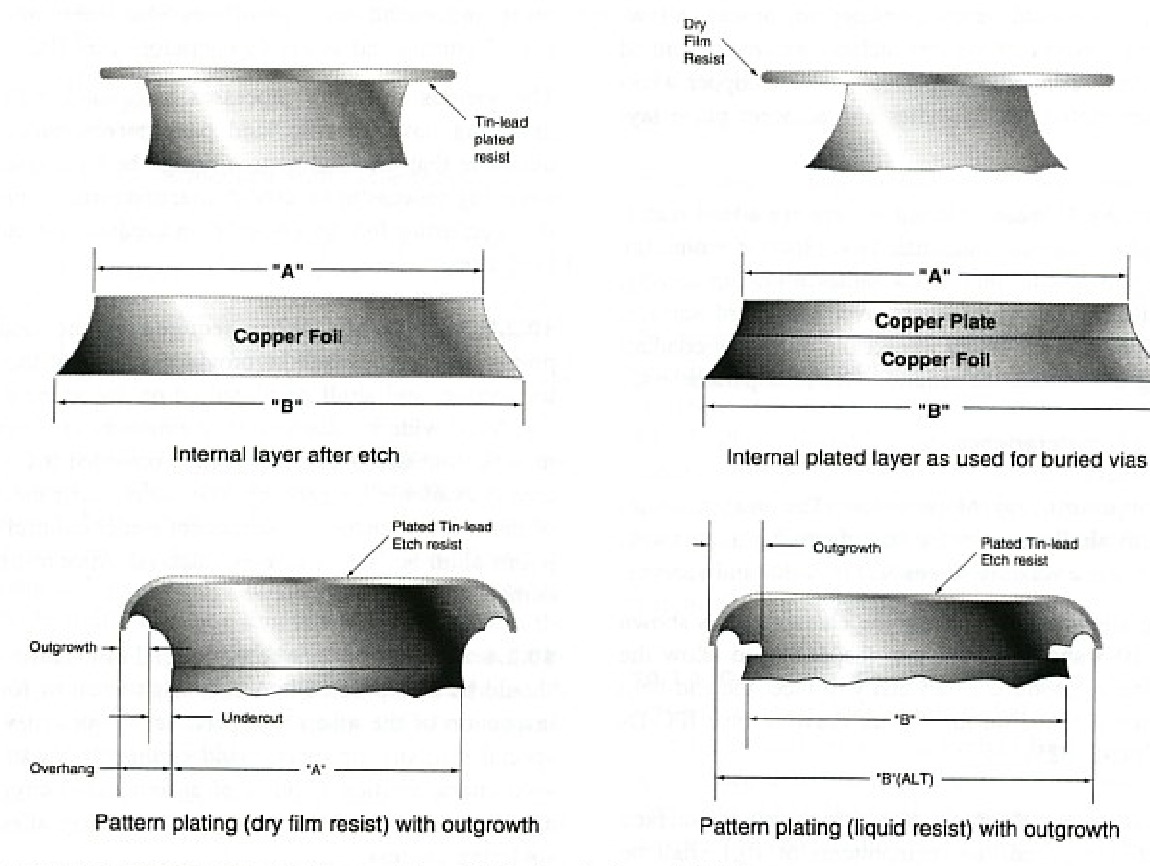
"A" POINT OF NARROWEST CONDUCTOR WIDTH: This is not "Minimum Conductor Width" noted on master drawings or performance specifications.

"B" CONDUCTOR BASE WIDTH: The width that is measured when "Minimum Conductor Width" is noted on the master drawing or performance specification.

"C" PRODUCTION MASTER WIDTH: The width usually determines the width of the metal or organic resist on the etched conductor.

Design width of the conductor is specified on the master drawing and is most often measured at the conductor base "B" for compliance to "minimum conductor width" requirements.

The following two configurations show that conductor width may be greater at the surface than at the base.



Internal layer after etch

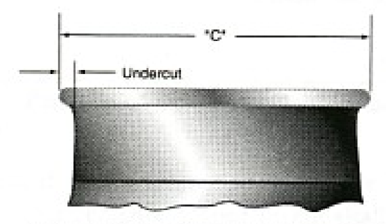
Internal plated layer as used for buried vias

Pattern plating (dry film resist) with outgrowth

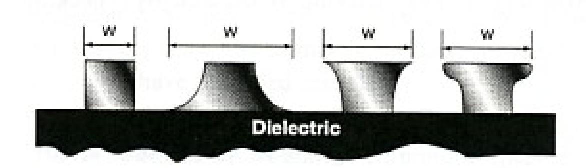
Pattern plating (liquid resist) with outgrowth

Note: The extent of outgrowth, if present, is related to the dry film resist thickness. Outgrowth occurs when the plating thickness exceeds the resist thickness.

"B" (ALT) would be used to determine compliance with "Minimum Conductor Width" for this etch configuration.



Thin clad & pattern plating (etch resist)



The effective width of a conductor may vary from the conductor width from surface obstructions (W).

Note: The different etch configurations may not meet intended design requirements.

IPC-2221a-10-03

Figure 10-3 Etched Conductor Characteristics

11 DOCUMENTATION

The printed board documentation package usually consists of the master drawing, master pattern drawing or copies of the artwork masters (film or paper), printed board assembly drawing, parts lists, and schematic/logic diagram.

The documentation package may be provided in either hard copy or electronic data. All electronic data **shall** meet the requirements of IPC-2510 series of standards.

Other documentation may include numerical control data for drilling, routing, libraries, test, artwork, and special tooling. There are design and documentation features/ requirements that apply to the basic layout, the production master (artwork), the printed board itself, and the end-item printed board assembly; all must be taken into consideration during the design of the board. Therefore it is important to understand the relationships they have with one another as shown in Figure 11-1.

The printed board documentation **shall** meet the requirements of IPC-D-325. In order to provide the best documentation package possible, it is important to review IPC-D-325 and identify all the criteria that are affected by the design process, such as:

- Parts information.
- Nonstandard parts information.
- Master drawing.
- Artwork masters production.
- Master pattern drawing.

11.1 Special Tooling During the formal design review prior to layout, special tooling that can be generated by the design area in the form of artwork or numerical control data **shall** be considered. This tooling may be needed by fabrication, assembly, or testing. Examples of such tooling are:

- Plots of numerical data to be used as check film.
- Buried or blind via land masters to assist in determining the location of the vias during layer fabrication for composite printed boards.
- Via land masters for composite printed boards to assist in distinguishing between vias that are to be drilled before lamination and vias that will be drilled after lamination.
- Artwork overlays to provide aids such as drill origin, spotter lands for nonplated through-holes without lands on the artwork, printed board coordinate zero, printed board profile, coupon profile, or profile of internal routed areas.
- Artwork for solder resist stripping which is used in some processes for solder mask over bare copper. The artwork should be designed to allow a solder resist overlap onto the solder at the copper/solder interface.
- Artwork overlays that can be used in assembly to assist with component insertion.
- Numerical data for auto-insert equipment at assembly.
- Solder paste stencil data.

11.2 Layout

11.2.1 Viewing The layout should always be drawn as viewed from the primary side of the board. For phototool generation purposes, the viewing requirements **shall** be identical to the layout (see IPC-D-310).

The definition of layers of the board **shall** be as viewed in Figure 11-2. Distinguishing characteristics **shall** be used to differentiate between conductors on different layers of the board.

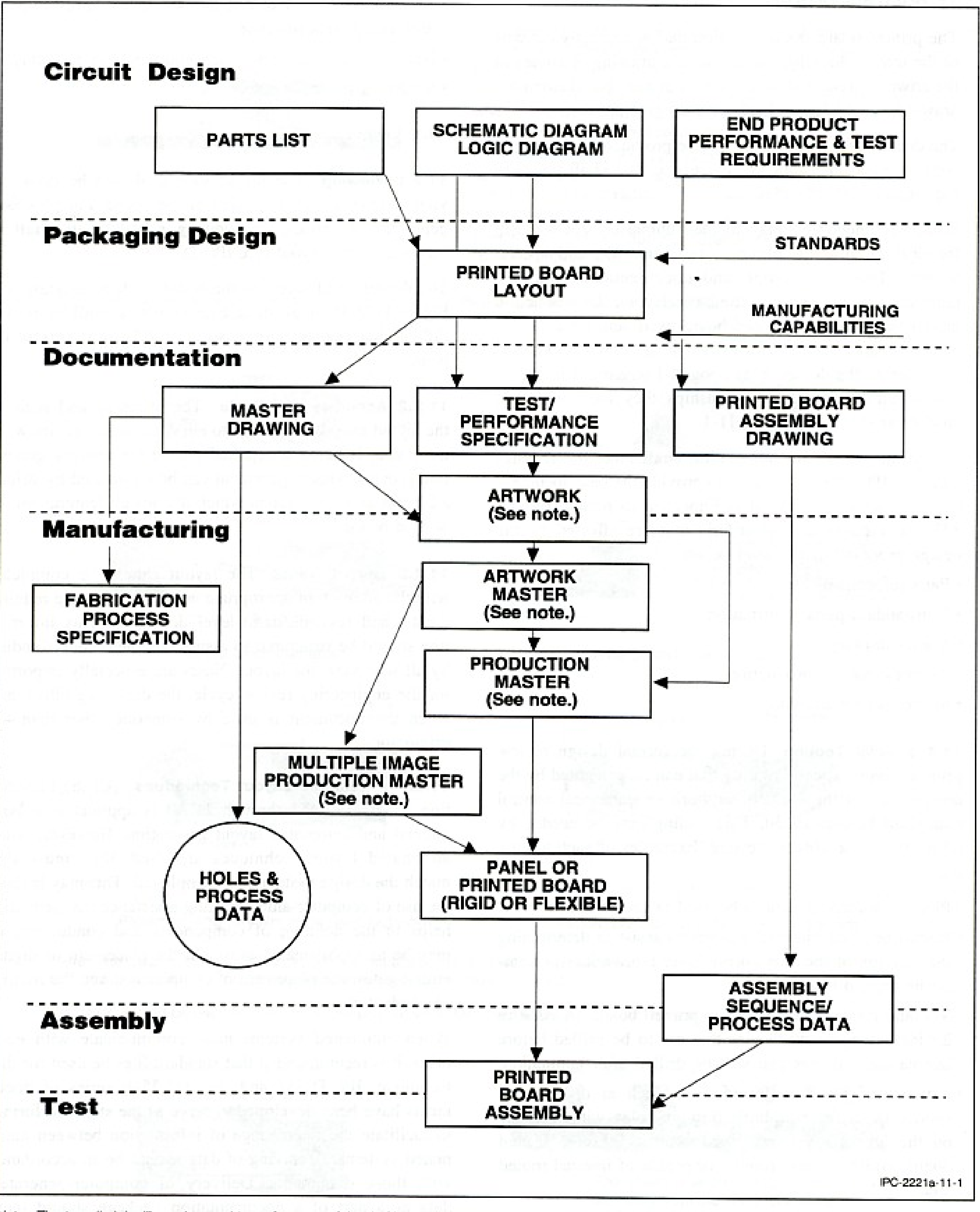
11.2.2 Accuracy and Scale The accuracy and scale of the layout must be sufficient to eliminate inaccuracies when the layout is being interpreted during the artwork generation process. This requirement can be minimized by strictly adhering to a grid system which defines all features on the printed board.

11.2.3 Layout Notes The layout should be completed with the addition of appropriate notations, marking requirements, and revision/status-level definition. This information should be structured to assure complete understanding by all who view the layout. Notes are especially important for the engineering review cycle, the digitizing effort, and when the document is used by someone other than the originator.

11.2.4 Automated-Layout Techniques All the information listed in 11.2.1 through 11.2.3 is applicable to both manual and automated layout generation. However, when automated layout techniques are used, they must also match the design system being employed. This may include the use of computer-aided drafting assistance that primarily helps in the defining of components and conductors, or may be as sophisticated as to add the placement of digital circuit gates, the placement of components, and the routing of conductors.

When automated systems must communicate with each other, it is recommended that standard files be used for this technique. IPC-D-356 and the IPC-2510 series of documents have been developed to serve as the standard format to facilitate the interchange of information between automated systems. Archiving of data should be in accordance with those documents. Delivery of computer-generated data as a part of a documentation package should meet these requirements.

With automated techniques, the data base should detail all the information that will be needed to produce the printed



Note: The term "original" may be used to preface any of the drafting and photographic tooling terms used in the figure. The "original" is not usually used in manufacturing processes. In the event a "copy" is made, the copy **shall** be of sufficient accuracy to meet its intended purpose if it is to take on the name of any one of the terms used in this figure. Other adjectives may also be used to help describe the kind of copy, e.g.: "nonstable," "first generation," "record," etc.

Figure 11-1 Flow Chart of Printed Board Design/Fabrication Sequence

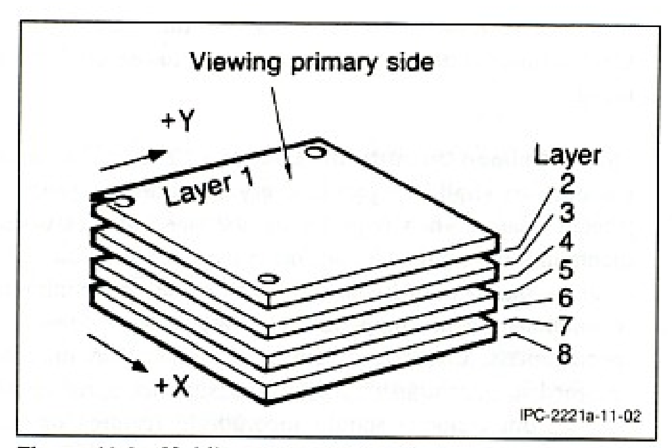


Figure 11-2 Multilayer Board Viewing

board. This includes all notes, plating requirements, board thickness, etc. A check plot should be employed to verify that the data base matches the requirements.

11.3 Deviation Requirements Any deviation from this standard or drawing **shall** have been recorded on the master drawing or a customer-approved deviations list.

11.4 Phototool Considerations The same land pattern configuration and nominal dimensions may be used for preparing the phototool for the stencil or screen used for solder paste application.

11.4.1 Artwork Master Files An electronic data file or alternative physical media, which defines the master image for each layer, that **shall** be provided as part of the master drawing set.

11.4.2 Film Base Material The artwork master, if supplied, **shall** be on a minimum of 0.165 mm [0.0065 in] thick biaxially oriented, dimensionally stable, polyester type film, or on glass photographic plates. Common film thickness ranges from 0.18 mm [0.007 in] to 0.28 mm [0.011 in]. Photographical glass plates range from 1.5 mm [0.0591 in] to 4.75 mm [0.190 in].

11.4.3 Solder Resist Coating Phototools Solder resist coating phototools may be prepared in two ways. The first method is to provide a special land pattern for each component using larger shapes to establish the solder resist clearance around the conductive pattern (see Figure 11-3). There may be other factors, such as fiducials, mounting holes and board edges which may require clearances.

The second method is to provide the same land pattern shapes for solder resist windows as used to establish the conductive pattern. In this method, the manufacturer of the printed board photographically expands the solder resist pattern to provide the necessary clearances. Thus, the same phototool may be used to establish the conductive pattern,

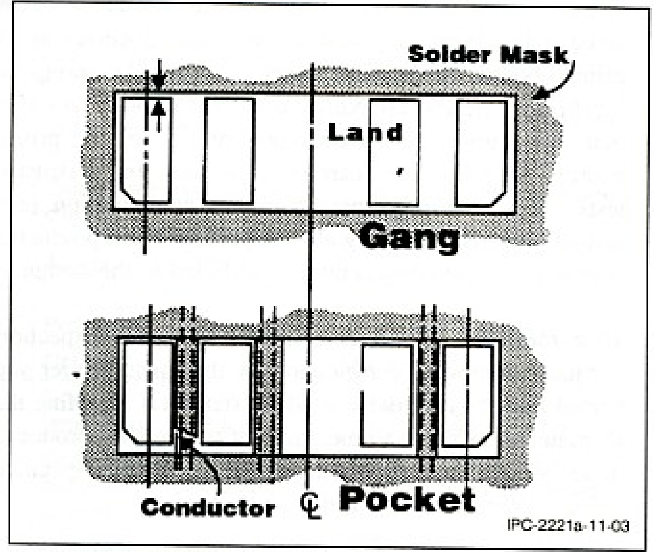


Figure 11-3 Solder Resist Windows

the solder resist openings, and the solder paste deposition tool. The ability to use the same phototool for the three processing steps enhances registration capabilities of the three image-dependent procedures and also keeps computer library symbol (land pattern) types to a manageable limit when computer aided design (CAD) systems are used. When utilizing this option, maximum clearance values must be specified on the master drawing.

12 QUALITY ASSURANCE

Quality assurance concepts should be considered in all aspects of printed board design. Quality assurance evaluations relating to design should consist of the following:

- Material.
- Conformance inspection.
- Process control evaluations.

This section defines the various coupons that should be considered during the design process. Also included is the rationale and purpose for the use of each coupon.

12.1 Conformance Test Coupons Conformance test coupons, when required, **shall** be in accordance with this section. Quality assurance provisions often require the use of specific test procedures or evaluations to determine if a particular product meets the requirements of the customer or specifications. Some of the evaluations are done visually, others are done through destructive and nondestructive testing.

Some quality evaluations are performed on test coupons because the test is destructive or the nature of the test requires a specific design which may not exist on the printed board. Test coupons are used in these types of tests as representatives of the printed boards fabricated on the same panel.

A test coupon is a suitable sample for destructive testing since it has been subjected to the same processes as the printed boards on the same panel; however, the design and location of the test coupons are critical in order to ensure that the coupons are truly representative of the printed boards. A production board may be used for destructive tests. Tests requiring specific circuit configuration (e.g., insulation resistance) may also be performed on production boards if appropriate circuitry is included in the design.

12.2 Material Quality Assurance Material inspections normally consist of certification by the manufacturer supported by verifying data based on statistical sampling that all materials which become a part of the finished product is in accordance with the master drawing, material specifications, and/or procurement documentation.

Conformance coupons are defined in the detailed specifications for the base material. As an example, copper foil is tested for tensile strength, ductility, elongation, fatigue ductility, peel strength, and carrier release strength. In most instances, the conformance test coupons for metal foil consist of a specific length and width.

Laminate specifications, however, require conformance coupons that relate more to performance of the end product board. Not only are peel strength, dielectric breakdown, and water absorption tested, the methods of examination require that specific coupon geometries be prepared in order to make the test as meaningful as possible. When a design requires verification of the base material at the end product board level, conformance coupons are used to establish that evaluation is identical or similar to those defined in existing base material specifications. Some users may require more than one ply of reinforcement and greater than 0.05 mm [0.0197 in] dielectric thickness. Example: Some military specifications require two ply reinforcement and greater than 0.09 mm [0.00354 in] dielectric thickness.

Each design sectional allows for a minimum dielectric thickness between layers of a multilayer printed board, when agreed upon between user and supplier. When this requirement is agreed upon, conformance test coupons must be provided as a part of the design to verify the specific resin and resin content, glass style, dielectric withstanding voltage between claddings and moisture resistance verification.

12.3 Conformance Evaluations Conformance evaluations are performed on production boards and/or conformance coupons. If a production board is selected for conformance evaluation, it should be capable of meeting the requirements of Table 12-1. Coupons required for conformance evaluation **shall** be as defined herein. Additional conformance coupons may be added by the manufacturer. Conformance coupons **shall** be traceable to the production panel.

12.3.1 Coupon Quantity and Location The conformance test circuitry **shall** be a part of every panel used to produce printed boards when required by the procurement documentation or applicable performance specification. The coupons outlined in Table 12-1 constitute the minimum requirements to be compatible with the most performance specifications. Coupons of custom configuration may be designed to accomplish specific user/supplier agreements. The custom coupons should incorporate features on the same dimensional plane to ensure compatibility with other standard coupons and the applicable performance specification.

All applicable configurations of test coupons **shall** be defined on the master artwork, the master drawing or added to the build artwork by the manufacturer to accommodate requirements of the performance specification. The location of the construction integrity coupons should be positioned within 12.7 mm [0.500 in] of the printed board profile to reflect build and plating characteristics. The recommended minimum number of coupons is defined in Table 12-1. Figure 12-1 shows an example of coupon location concepts. The fabricator may position the coupons to optimize panelization, tooling and material utilization. At least one hole in each coupon should be located on the same grid as the printed board features. When coupon retention is required for traceability it is recommended that an additional coupon set be ganged together in a common strip.

12.3.2 Coupon Identification Conformance test circuitry **shall** provide space for:

- Board part number and revision letter.
- Traceability identification.
- Lot date code.
- Manufacturer's identification, e.g., Commercial and Government Entity (CAGE), logo, etc.

Special coding systems may be used provided they are identified on the master drawing.

12.3.3 General Coupon Requirements Test coupons should reflect the specific board characteristics. This information consists of meeting the requirements for holes, conductors, spaces, etc. When coupons are used to establish process control parameters, they **shall** consistently use a single hole size or land configuration which reflects the process. Process characteristics and general board characteristics should be matched (e.g., threshold technology, leading edge technology, etc.).

Table 12-1 Coupon Frequency Requirements[1]

Coupon Purpose	I.D.[2]	Class 1	Class 2	Class 3
Conformance Testing				
Rework Simulation	A/B or A	Not required	Twice per panel	Twice per panel, opposite corners
Thermal Stress, Plating Thickness, and Bond Strength Type 1	A/B or A or B	Twice per panel, opposite corners	Twice per panel, opposite corners	Twice per panel, opposite corners
Thermal Stress, Inner Layer Interconnect Integrity	A or A/B	Not required	As agreed upon between user and supplier	Required
Hole Solderability	S[3]	Optional	Preferred, 1 per panel	Preferred, 1 per panel
Hole Solderability	A/B or A	Not Required	Optional	Optional
Solder Resist Tenting (if used)	T	Not required	Once per panel with solder resist, location optional	Once per panel with solder resist, location optional
Peel Strength	C	Not required	Once per panel, location optional, pattern defined by artwork	Once per panel location optional, pattern defined by artwork
Solder Resist (if used)	G	Once per panel with solder resist, location optional	Once per panel with solder resist, location optional	Once per panel with solder resist, location optional
Surface Mount Solderability (Optional for SMT)	M	Not required	Once per panel, location optional, pattern defined by artwork	Once per panel, location optional, pattern defined by artwork
Reliability Assurance Inspection				
Peel Strength, Surface Mount Bond Strength (Optional for SMT)	N	Not required	Once per panel, location optional, pattern defined by artwork	Once per panel, location optional, pattern defined by artwork
Surface Insulation Resistance	H	Once per panel, location optional	Twice per panel, opposite corners	Twice per panel, opposite corners
Moisture and Insulation Resistance	E	Once per panel, location optional	Twice per panel, opposite corners	Twice per panel, opposite corners
Optional or Process Control				
Registration (Option 1 or 2)	F	Not required	Four per panel, opposite sides defined by artwork	Four per panel, opposite sides defined by artwork
Registration (Optional)	R	Not required	Four per panel, opposite sides defined by artwork	Four per panel, opposite sides defined by artwork
Interconnect Resistance (Option 1 or 2)	D	Not required	Once per panel, location optional, pattern defined by artwork	Once per panel, location optional, pattern defined by artwork
Bending Flexibility, Flexible Endurance	X	Optional, pattern defined by artwork	Optional, pattern defined by artwork	Optional, pattern defined by artwork

1 If additional coupons for impedance testing are required, follow guidelines of IPC-D-317 and IPC-2141.
2 Where possible, coupon identification letters have been chosen to conform to those currently being used for conformance evaluations.
3 See IPC-J-STD-003.

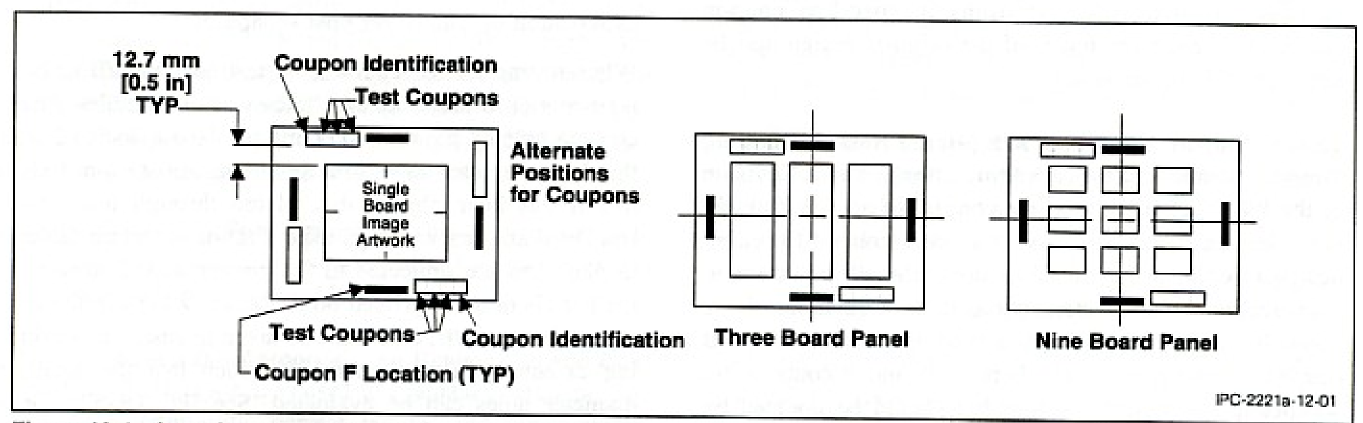


Figure 12-1 Location of Test Circuitry

12.3.3.1 Tolerances Tolerances for the fabrication of test coupons **shall** be the same as those for the printed board.

12.3.3.2 Etched Letters Etched letters shown on coupons are for reference only.

12.3.3.3 Interlayer Connection Holes Whenever a multilayer design incorporates interlayer connection holes in the form of blind or buried vias, Coupons A, B, and D **shall** be designed so as to incorporate these types of holes connecting the appropriate layers. The individual coupon description contains information on how these holes are to be incorporated. The specific number of holes for evaluation should be a minimum of three in each individual test coupon with a minimum of two test coupons required on each individual panel.

12.3.3.4 Metal Cores Whenever a multilayer design uses metal cores, the same core(s) **shall** be incorporated into the design of the coupon.

If the metal core(s) has interlayer connection holes that pass through the core without contact, the design of the coupon **shall** be representative of that characteristic. If the hole contacts the core, that characteristic **shall** also be represented in the coupon. The minimum number of holes for this evaluation are three per coupon with a minimum of two coupons on each individual panel. Additional A and B coupons may be required for horizontal microsections.

Composite printed boards **shall** have separate coupons for the top side board, the bottom side board, and the composite board. The coupon for the composite printed board **shall** include the core material.

12.4 Individual Coupon Design Individual test coupons are designed to evaluate specific individual characteristics of the printed boards they represent. Appropriate master drawings IPC-100103 and IPC-100043 are provided through the IPC-A-47 and IPC-A-43 artwork phototool packages, respectively. Variations in specified coupon design must meet the intent of the original design and be representative of the board.

12.4.1 Coupon A and B or A/B (Plated Hole Evaluation, Thermal Stress and Rework Simulation) The A Revision of the IPC-2221 introduced the concept of an A/B coupon. It has been generated to provide a single coupon for either designers or those board fabricators who do not want to microsection two separate coupons to view small and large holes. It incorporates most aspects of the heritage A and B coupons in one coupon. The heritage A and B coupons are acceptable for existing designs but should be updated by the manufacturer when practical. The second row of holes within the A/B coupon provides a single view of small and large holes for PTH evaluation and thermal stress. The outer row provides for rework simulation of component holes.

These coupons are used to evaluate plated holes as established in the applicable performance specification. Figures 12-2 and 12-4 show the general configuration of the coupons for through holes. A conductor may be included in between the small holes on the external layer of the coupons. These surface conductors are provided as assistance for coupon mounting and to maintain/confirm axis orientation post grinding and provide planar information only. It is recommended that they should not be used for conductor quality verification purposes. The pad/hole relationship **shall** represent the design within the coupon except that the design attributes fall outside the min/max configuration illustrated in Figure 12-4. In this situation, choose the next available size employed in the design. Imaged layers **shall** represent printed circuit board design, e.g., pad size and plane layers, except that nonfunctional lands **shall** be included on all layers for purposes of construction integrity analysis such as registration, annular ring, post separation interconnect, etc. Layer numbers are positioned throughout the coupon to indicate axis orientation when optional horizontal mounting and grinding is employed. The layer numbering will be offset on each successive layer to prevent buildup as indicated in Figure 12-4.

Thermal Stress testing is used to indicate innerlayer separations or barrel cracking. It is necessary to subject both component holes and vias to this test.

When testing for rework simulation, test coupon A/B or heritage coupon A **shall** contain holes with the largest diameter component hole on the printed board and land associated with that hole diameter that can be fitted on a 2.54 mm [0.100 in] grid to a maximum hole size of 1.905 mm [0.075 in]. It has been shown that plated holes with large diameters are more susceptible to innerlayer separation as a result of higher radial tensile stresses and bending moments acting on the innerlayer interconnects near the surfaces of printed boards. See IPC-TR-486 for a detailed explanation on innerlayer post separation.

When testing for barrel cracking, test coupon A/B or heritage coupon B **shall** contain holes with the smallest diameter via hole on the printed board and land associated with that hole diameter down to a minimum of 0.15 mm [0.006 in]. It has been shown that plated through holes with smaller diameters and high aspect ratios are more difficult to plate and are subjected to the greater tensile stresses in the barrels near the printed board central z axis. In the case of test coupon A/B, care must be taken to ensure that grinding extends past the outer holes such that the smallest diameter holes can be evaluated. See IPC-TR-579 for a detailed explanation on the reliability of small diameter holes. The coupon outline border on layer one is optional

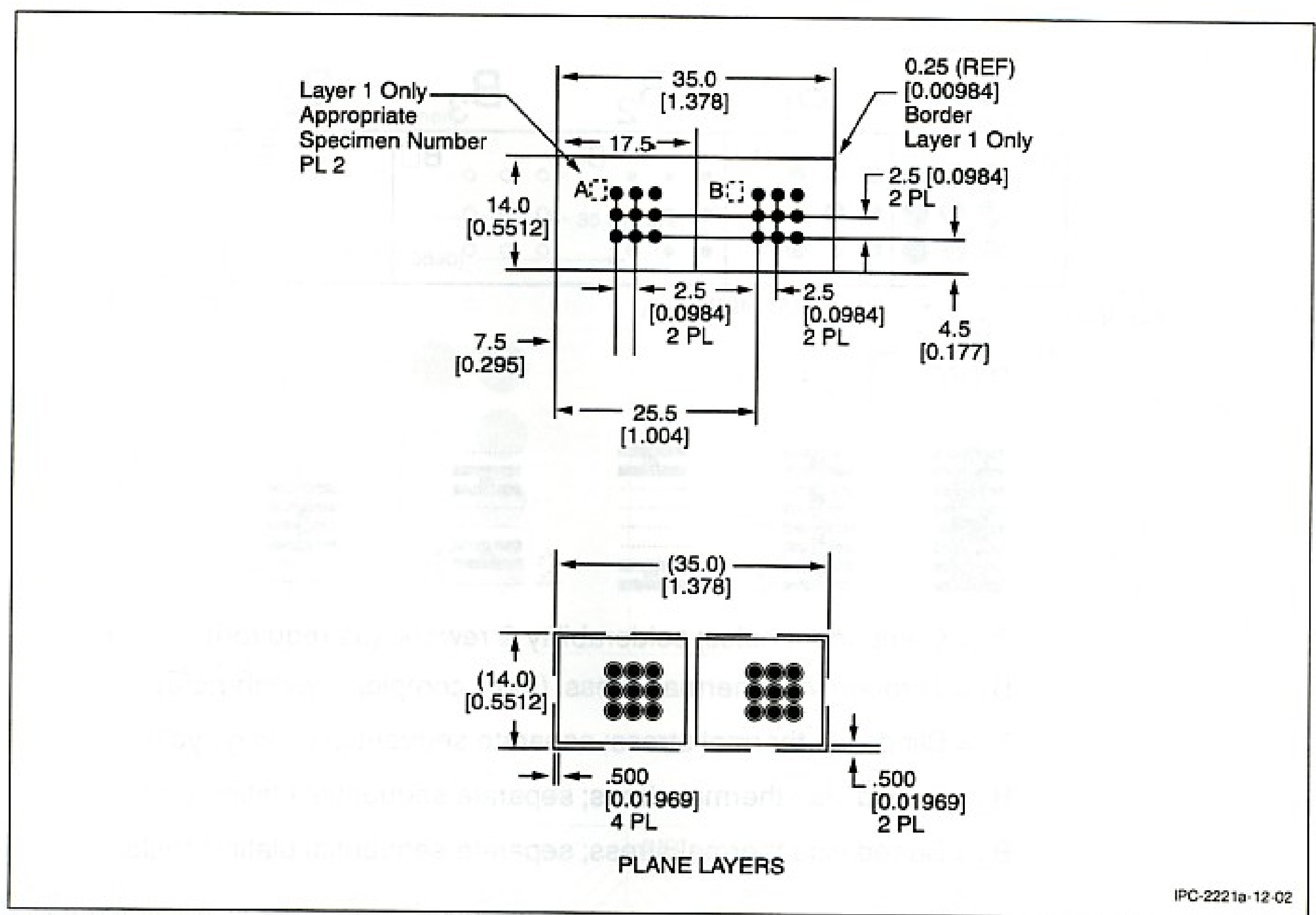


Figure 12-2 Test Coupons A and B, mm [in]

and may be produced by screening or etch. The border may be solid or segmented in order to accommodate placement of tooling holes for automated polishing equipment.

For blind and buried via interconnects, a minimum of one additional heritage B or A/B coupon **shall** be added to represent the most complex build construction. See Figure 12-3 for an example of additional heritage B coupon use and Figure 12-5 for an example of additional A/B coupon use.

Note: Coupon S is preferred for component hole solderability testing (see 12.4.9 and Figure 12-20). Coupon A/B or heritage coupons A and B are not required for nonplated-through hole SMT designs (see 12.4.7 and Figure 12-7). Figures 12-2 and 12-4 illustrate typical clearance areas in plane areas per the design minimum.

12.4.2 Coupon C (Peel Strength) This coupon is used to evaluate peel strength of metallic foils. The design of this coupon is shown in Figure 12-6.

12.4.3 Coupon D (Interconnection Resistance and Continuity) Test coupon D is used to evaluate interconnection resistance, continuity, correct lay-up, and other performance criteria. See Figure 12-7 for an example of coupon D. Figure 12-8 shows the modification to be made to coupon D for buried vias.

12.4.3.1 Conformance Testing For conformance testing, the number of layers, lay-up, layer configuration, and use of nonfunctional lands **shall** be modified to reflect the board design. The land size **shall** be representative of the board and the hole diameter **shall** be the smallest in the associated board with the exception of A1, A2, B1, and B2 which **shall** be a minimum of 0.75 mm [0.0295 in]. Since the smallest hole represents the most difficulty in meeting plating requirements, this will ensure that the evaluation of the D coupon parallel the characteristic with the most variability. The length of the coupon will vary with the number of layers.

A typical example of a ten-layer, coupon D modified to include blind and buried vias is shown in Figure 12-7 and Figure 12-8. In general, the conductor **shall** be continuous from holes A1/A2 to holes B1/B2 and **shall** be arranged symmetrically around the centerline of the coupon.

The conductors **shall** not be routed stepwise through the coupon, but rather arranged so that the interconnects in a specific hole are separated to the greatest extent possible. The maximum number of holes in the coupon are not

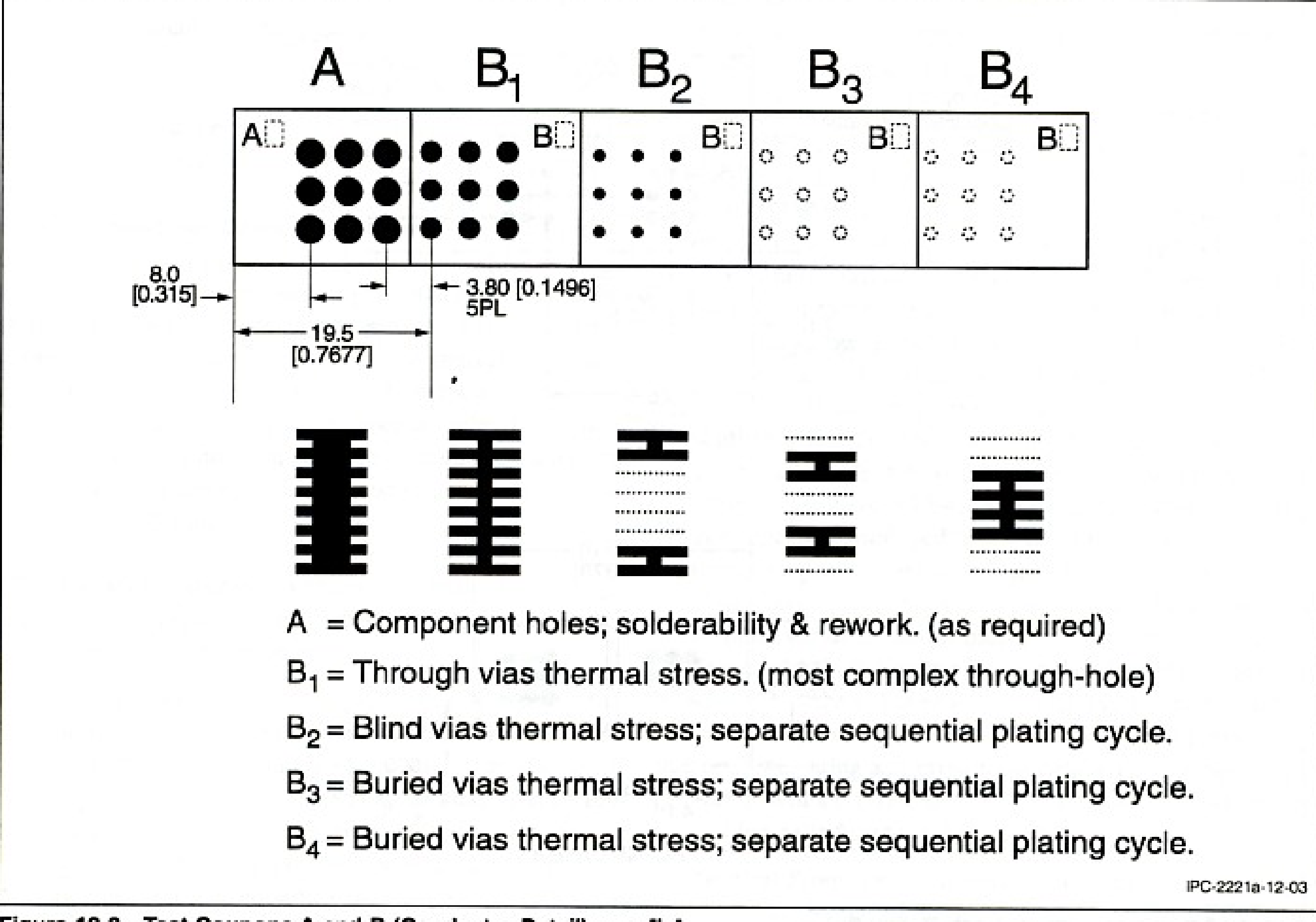


Figure 12-3 Test Coupons A and B (Conductor Detail) mm, [in]

restricted; however, the minimum number of holes **shall** be two times the number of layers plus four (for holes A1, A2, B1, and B2).

Except for plane layers, there **shall** be a minimum of two conductor paths for each layer of the printed board design, one on each side of the centerline. If there are no conductors on the external layers, the connections **shall** be moved to layer 2 and layer n-1 respectively.

With the exception of the layer 1 conductors connecting holes A1/A2 to 01 and B1/B2 to 24, respectively, the conductor width on each layer **shall** be the minimum used on that layer of the printed board design. The conductors on layer 1 used to establish connection to holes 01 and 24 must be of sufficient size to accommodate the 0.75 mm [0.0295 in] hole diameter for A1/A2 and B1/B2, and to allow for the attachment of source wiring of the precision resistance measurement equipment. Constraining cores and plated layers **shall** represent printed board design, e.g., ground ties on specific layers, deleted nonfunctional lands, etc. Blind and buried vias **shall** be included in the coupon design.

12.4.3.2 Process Control See Figure 12-9 as an example of a process control coupon.

12.4.4 Coupons E and H (Insulation Resistance) These coupons are used for evaluating insulation resistance, bulk resistance and cleanliness of the material after exposure to an elevated cyclic temperature and humidity under an applied voltage. The coupon can also be used for evaluating dielectric withstanding voltage.

The design of the coupon **shall** be in accordance with Figure 12-10 or Figure 12-11 except as noted below. The minimum land hole diameter **shall** be any leaded component hole or, if there are no component holes, the minimum land hole diameter **shall** be 0.50 mm [0.020 in]. The holes **shall** be left open. A pair of holes and a pair of conductors **shall** be provided for all layers of the coupon.

When using surface mount patterns, alternate coupons may be used to evaluate both insulation resistance and cleanliness of the bare board before and after solder resist. The "Y" pattern of coupon E can provide a useful tool for cleanliness and insulation resistance property evaluations. As in most instances, the coupon under large surface mount devices should be a comb pattern. Figure 12-12 shows several comb pattern combinations to evaluate land patterns used for surface mounting. These coupons and concepts may be incorporated directly on the board in a spare position for a component, or may be incorporated as conform-

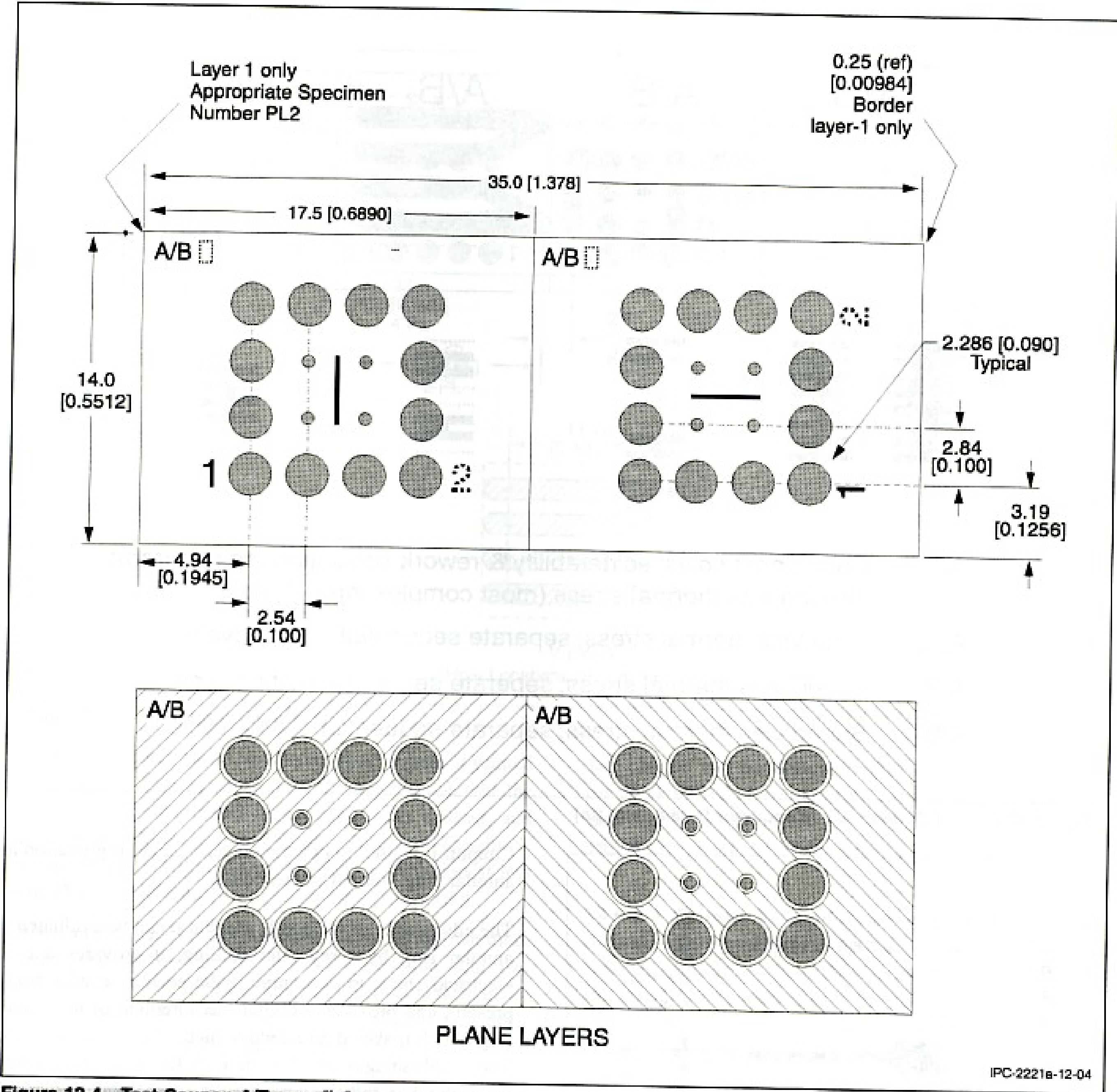


Figure 12-4 Test Coupon A/B, mm [in]

ance coupons on the panel for evaluation when assembling surface mount component in panel format. If a "Y" pattern is assigned to a chip component, the position can be left empty or can be filled to reflect cleanliness/insulation resistance properties of the bare board, or cleanliness/insulation resistance properties of the assembly (see Figure 12-13).

12.4.4.1 Coupon E Coupon E is used for general testing purposes. It is less sensitive to dirt and ionic contaminants. The general design of the coupon is shown in Figure 12-10.

12.4.4.2 Coupon H Coupon H is used for higher level insulation testing, such as telecommunications. See Figure 12-11 for typical design. The comb pattern requires more intensive cleaning process. This coupon is not referenced in IPC-6012. If it is used, the test method and performance criteria **shall** be specified in the procurement documentation.

12.4.5 Registration Coupon The purpose of the registration coupon is to evaluate the internal annular ring. When coupons A and B or A/B are used for registration evaluation, the technique requires multiple microsections. i.e., both x and y axes.

Figure 12-14 and Figure 12-15 dimensions apply to qualification testing only.

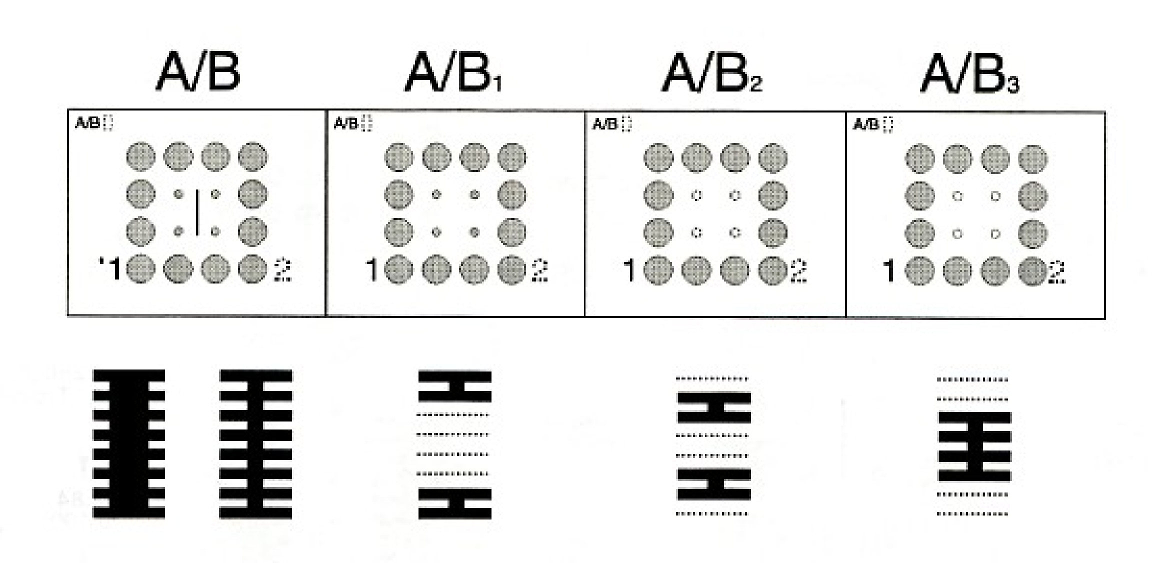


Figure 12-5 Test Coupon A/B (Conductor Detail), mm [in]

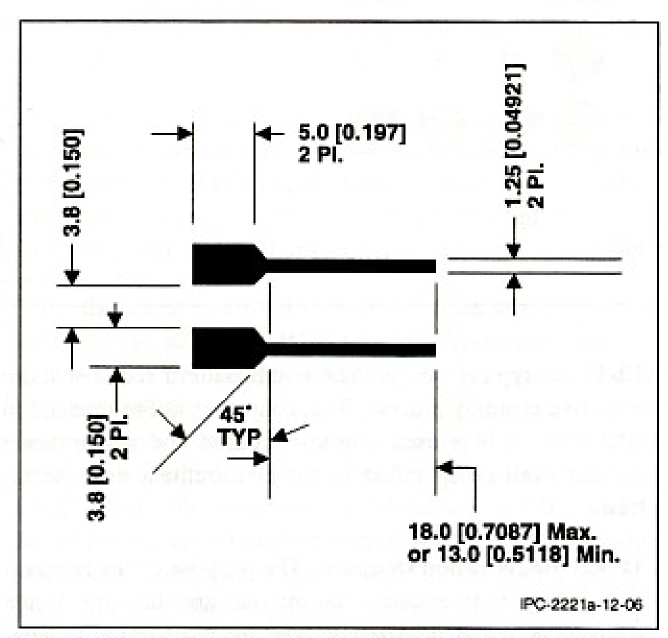


Figure 12-6 Coupon C, External Layers Only, mm [in]

Coupon F is used to evaluate layer-to-layer registration and annular ring without microsection.

The advantages of coupon R are that it can be evaluated for annular ring by x-ray after drilling, it provides a quick electrical check to determine if the correct annular ring is present, and provides a digital measurement of the annular ring which makes it an effective method of process control. The disadvantages are that the etch factor must be known for each layer, the x-ray must have a resolution of less than 25 µm [0.984 mil], a separate land must be present for each layer, and the coupon cannot be evaluated electrically until after the holes are plated.

Either F or R, or a combination, may be used to evaluate misregistration of the layers. The coupon **shall** be placed close to the board at the edge of the panel, near the center of the horizontal or vertical edge since that is where the most material movement occurs (see Figure 12-1).

12.4.5.1 Coupon F, Conformance Testing (Option 1) The design of the coupon **shall** be in accordance with Figure 12-14 with the hole diameter at the option of the manufacturer. The land size for this option includes an annular ring.

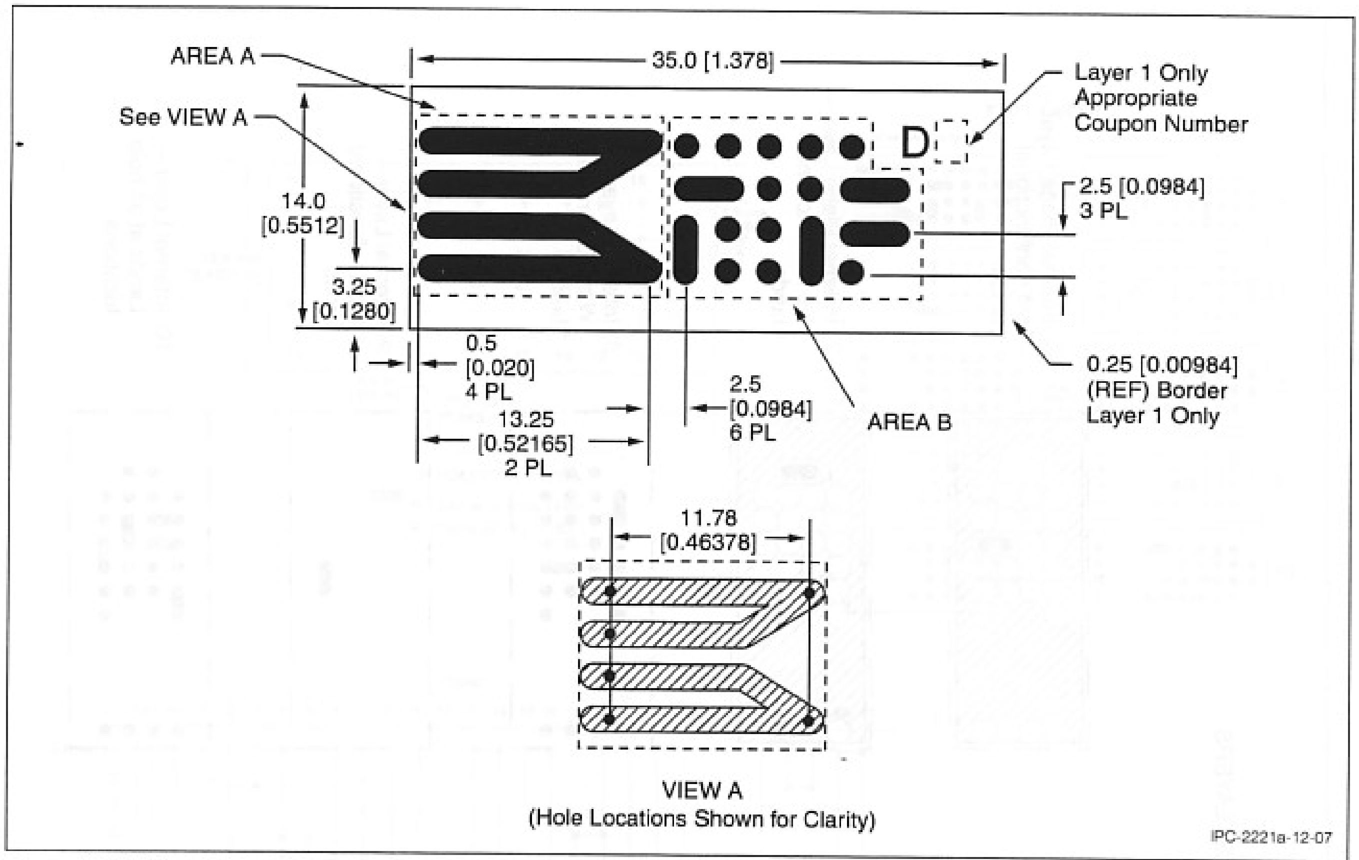


Figure 12-7 Test Coupon D, mm [in]

Constraining cores and plated layers **shall** represent printed board design. The advantages to this option are that the coupon may be evaluated immediately after drilling, and the etch factor does not need to be considered. The disadvantage is that it requires an x-ray with a resolution of less than 25 μm [0.984 mil] to measure the annular ring.

This concept places a land on every layer. If the manufacturer wishes to use another hole diameter, the land size **shall** be calculated for each internal layer separately using the formula in 9.1.1. The coupons are evaluated after drilling by measuring the annular ring using x-ray.

12.4.5.2 Coupon F, Conformance Testing (Option 2) The design of the coupon **shall** be in accordance with Figure 12-14 with the hole diameter at the option of the manufacturer. The land size for this option does not include an annular ring. Constraining cores and plated layers **shall** represent printed board design. This is the preferred coupon. The advantages to this option are that the coupons may be evaluated after drilling by x-ray for breakout, evaluation may be after etchback or hole clean using a visual inspection, and the etch factor need not be considered.

This concept places a land on every layer. If the manufacturer wishes to use another hole diameter, the land size **shall** be calculated for each internal layer separately using the formula in 9.1.1.

The coupon can be evaluated after drilling by inspecting for breakout using x-ray, or the coupon can be inspected after hole clean or etchback for a continuous ring in the drilled hole using a back-lit table.

12.4.5.3 Coupon R, Conformance Testing A typical coupon design is shown in Figure 12-15. The hole size and external lands are at the option of the fabricator. On internal layers, the coupon uses a ten hole pattern on 2.5 mm [0.0984 in] centers through a copper plane with circular clearance areas around nine of the holes. The clearance diameters are stepped in 0.05 mm [0.0197 in] increments for the first nine holes. There is no clearance area for the tenth hole so that the hole will make contact with the plane. The center clearance area **shall** be designed for the worst case hole-to-pad diameter difference for the layer. Since the manufacturing allowance may vary from layer-to-layer, see Figure 12-16, the diameter of the artwork center clearance area **shall** be calculated for each internal layer separately as follows:

Clearance diameter = nominal drilled hole diameter + manufacturing allowance

Manufacturing allowance = smallest difference between any functional plated hole and land on that layer - 2X annular ring.

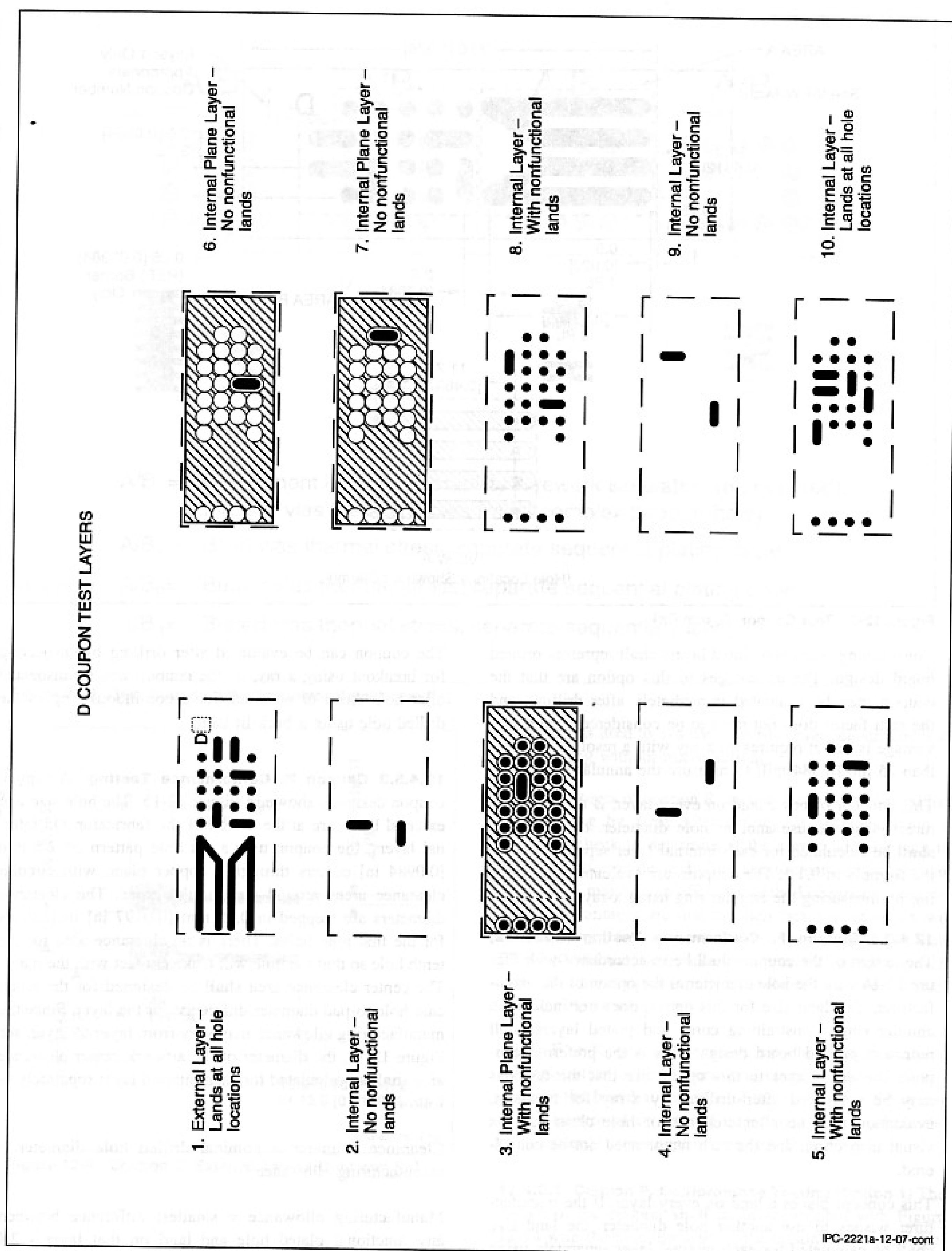


Figure 12-7 cont. 10 Layer Example

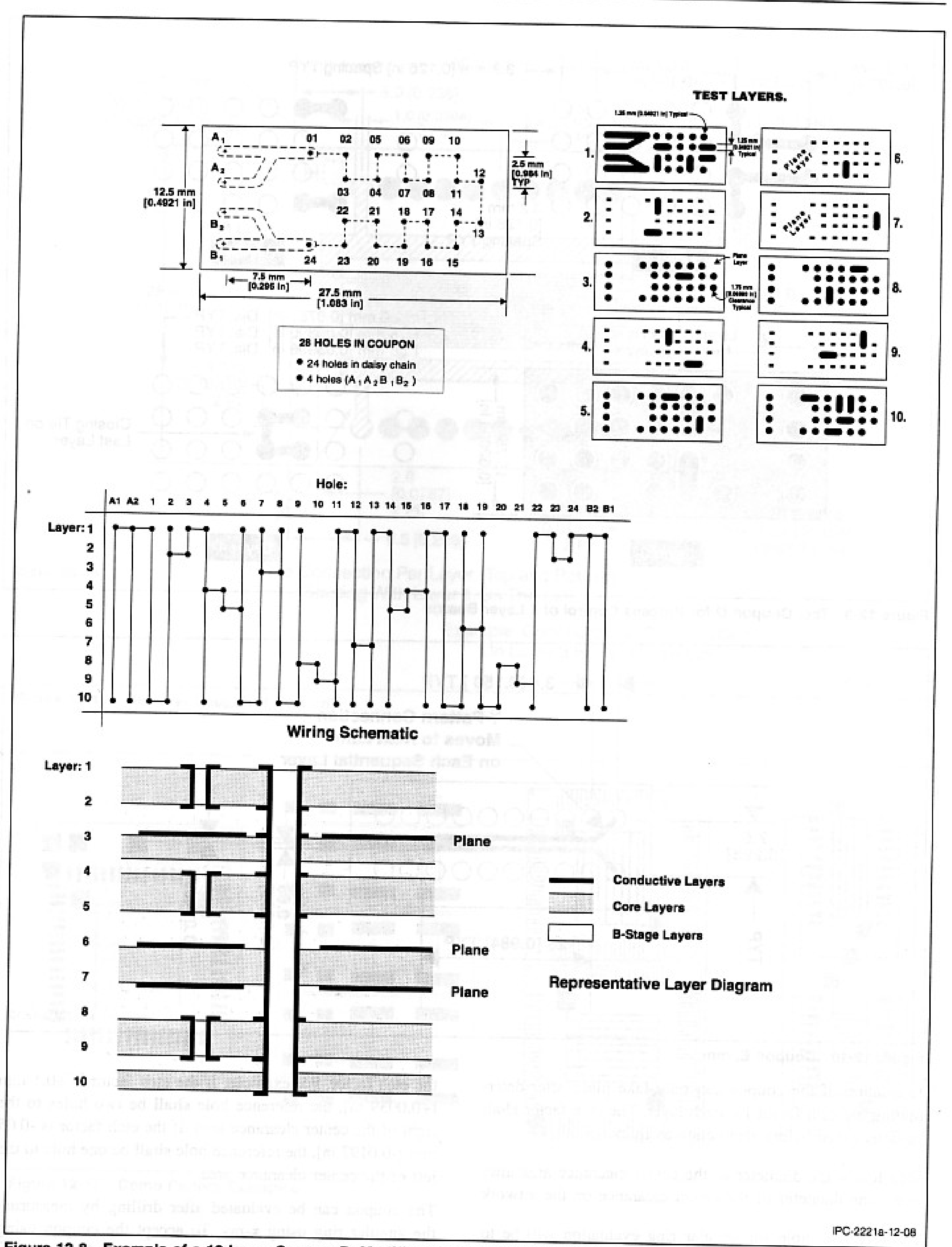


Figure 12-8 Example of a 10 Layer Coupon D, Modified to Include Blind and Buried Vias

5.0 mm [0.197 in]
5.0 mm [0.197 in]
3.2 mm [0.126 in] Spacing TYP
3.2 mm [0.126 in] Spacing TYP
Layer 1
Layer 2
Length Depends on Number of Layers
15.75 mm [0.62008 in]
Layer 3
2.0 mm [0.0787 in] Dia. TYP
1.75 mm [0.06890 in] Dia. TYP
1.50 mm [0.05906 in] Dia. TYP
Closing Tie on Last Layer
Layer 4
IPC-2221a-12-09

Figure 12-9 Test Coupon D for Process Control of 4 Layer Boards

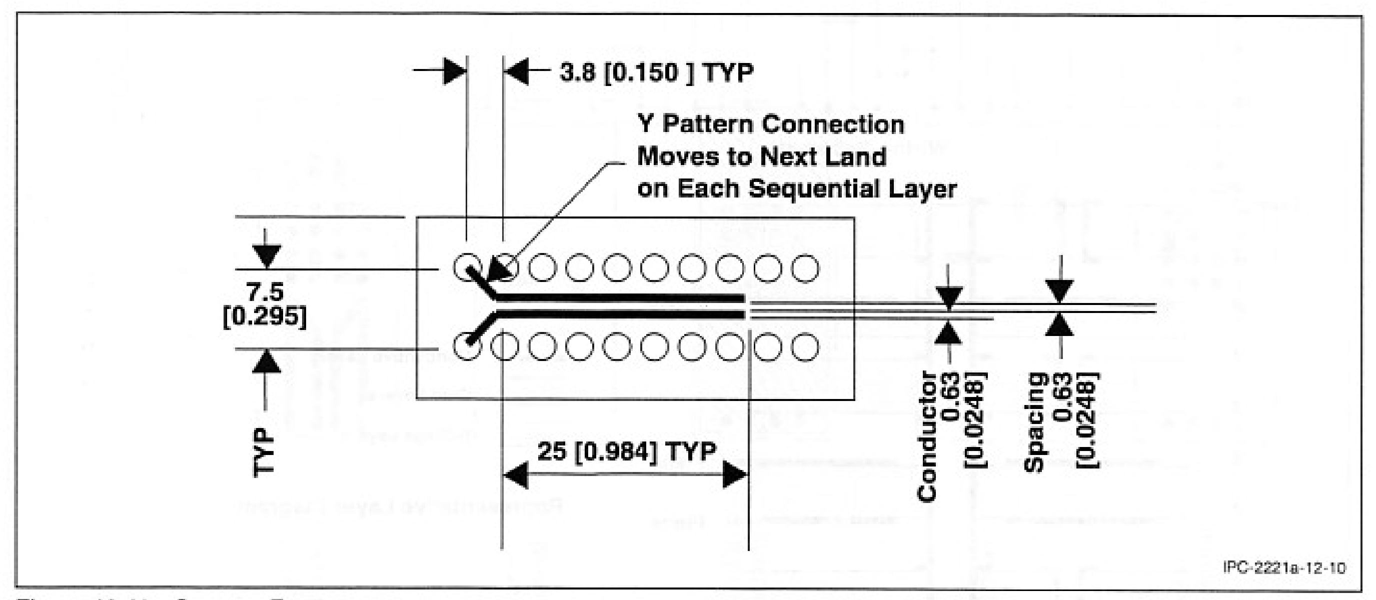


Figure 12-10 Coupon E, mm

Evaluation of the coupon can only take place after determining the etch factor for each layer. The etch factor **shall** be determined before lamination as follows:

Etch loss = the diameter of the center clearance area after etch - the diameter of the center clearance on the artwork

The reference hole for annular ring evaluation will be to the left or the right of the center clearance area based on the etch factor. For example: If the etch factor is +0.1 mm [+0.0039 in], the reference hole **shall** be two holes to the right of the center clearance area. If the etch factor is -0.05 mm [-0.0197 in], the reference hole **shall** be one hole to the left of the center clearance area.

The coupon can be evaluated after drilling by measuring the annular ring using x-ray. To accept the coupon using x-ray, the reference hole **shall** not touch the plane.

35.0 [1.378]
Layer 1 Only
Appropriate
Coupon Number
6.0 [0.236]
1.0 [0.0394]
2 PL
2.5
[0.0984]
18 PL
1.4 [0.0551]
Land Diameter
20 PL
1.0 [0.0394]
10 PL
H
DIM C
9 PL
2.0 [0.0787]
2 PL
28.0
[1.102]
DIM B
10 PL
3.375
[0.13287]
2 PL
1.0 [0.0394]
2PL
DIM A
2 PL
2.0
[0.0787]
2 PL
2.0
[0.0787]
2 PL
0.25 [0.00984]
(REF) Border
Layer 1 Only
6.5 [0.256]
One Connection Per Layer (Top and Bottom)
Starting With Layer 1 On The Left
Example: Connection To Comb Pattern
On Layer 3 Is Third From Left
IPC-2221a-12-11

Figure 12-11 Optional Coupon H, mm [in]

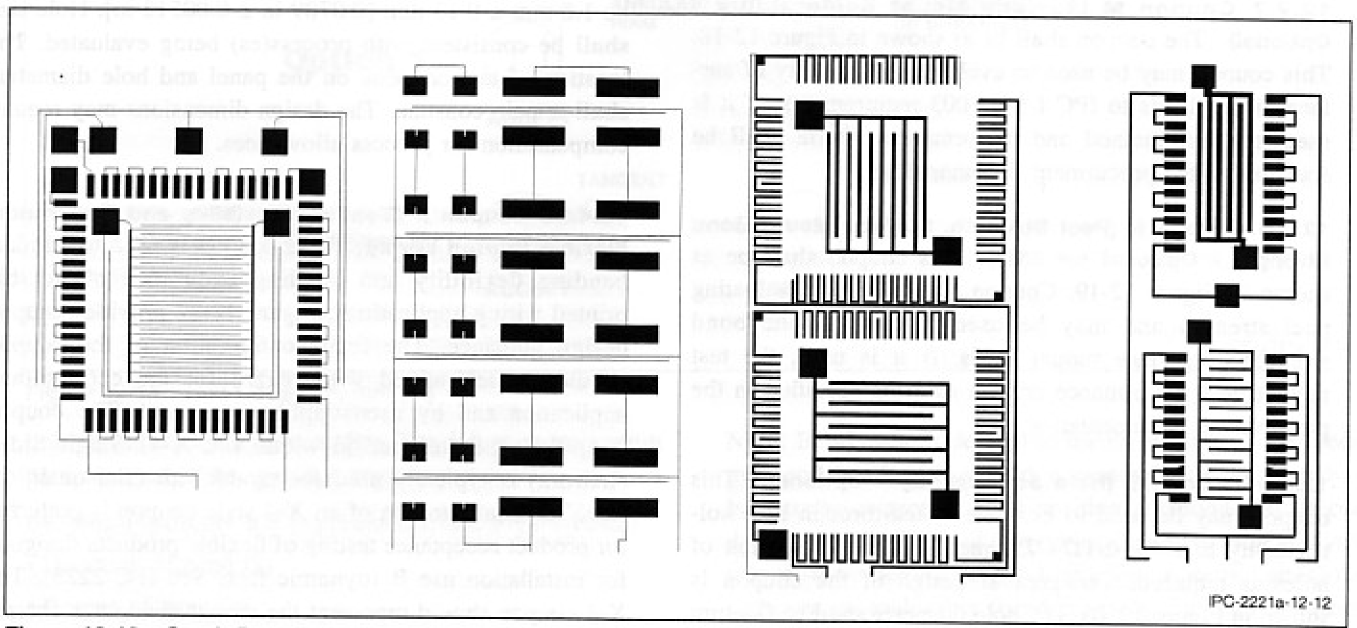


Figure 12-12 Comb Pattern Examples

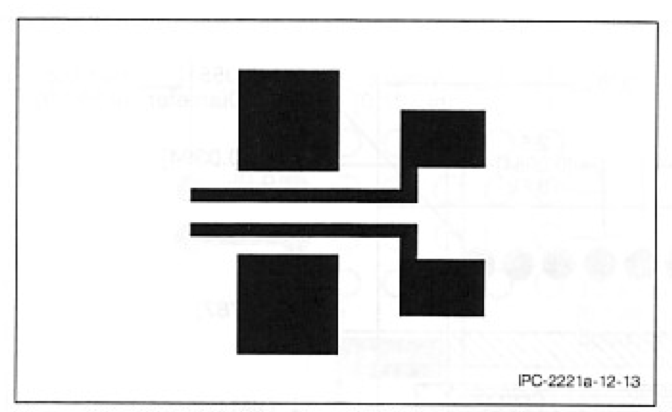


Figure 12-13 "Y" Pattern for Chip Component Cleanliness Test Pattern

The coupons are designed to measure annular ring after the holes are plated. The coupons are acceptable if there is no electrical connection between the reference hole and the tenth hole. The dimension of the annular ring can be determined by finding the first hole which makes electrical connection to the tenth hole and noting its position in relation to the reference hole. Each hole to the left or right of the reference hole represents a +25 µm [+0.984 mil] or -25 µm [-0.984 mil] respectively to the reference annular ring. This coupon is not referenced in IPC-6012. If it is used, the test method and performance criteria **shall** be specified in the procurement documentation.

12.4.6 Coupon G (Solder Resist Adhesion) The test coupon for evaluating solder resist adhesion **shall** be as shown in Figure 12-17. The artwork **shall** provide for solder resist to cover the entire coupon.

12.4.7 Coupon M (Surface Mount Solderability - Optional) The coupon **shall** be as shown in Figure 12-18. This coupon may be used to evaluate solderability of surface mount lands to IPC-J-STD-003 requirements. If it is used, the test method and performance criteria **shall** be specified in the procurment documentation.

12.4.8 Coupon N (Peel Strength, Surface Mount Bond Strength - Optional for SMT) This coupon **shall** be as shown in Figure 12-19. Coupon N is used for evaluating peel strength and may be used to evaluate the bond strength of surface mount lands. If it is used, the test method and performance criteria **shall** be specified in the procurement documentation.

12.4.9 Coupon S (Hole Solderability - Optional) This coupon may be used to evaluate plated-through hole solderability to IPC-J-STD-003 when a larger population of holes is required. The general design of the coupon is shown in Figure 12-20. The hole diameter **shall** be 0.8 mm ± 0.13 mm [0.031 in ± 0.00512 in] required to be solder filled. If it is used, the test method and performance criteria **shall** be specified in the procurement documentation.

12.4.10 Coupon T This coupon **shall** be used to validate tenting characteristics when solder resists are used to tent plated-through holes (see 4.5.1). Coupon T is the same as shown in Figure 12-20 (coupon S) except that the entire coupon **shall** be covered with solder resist on both sides.

The hole diameter **shall** be the largest plated hole which will be tented with solder resist. This coupon is not referenced in IPC-6012. If it is used, the test method and performance criteria **shall** be specified in the procurement documentation.

12.4.11 Process Control Test Coupon Process control test coupons are used at strategic points in the process flow to evaluate a specific process or set of processes. The designs of the process control test coupons are at the option of the printed board fabricator. Each design is specific to the processes for which the fabricator intends to evaluate.

Process control evaluations are established through a systematic path for implementing statistical process control. This includes those items shown in Figure 12-21.

If the contract permits the use of process control coupons in lieu of conformance coupons, the design of the coupon **shall** be agreed to between the user and manufacturer.

The design of existing test coupons can serve as a guide for the design of process control test coupons. In general, the design of the coupon is consistent with the process to be evaluated rather than an attempt to represent a printed board design. Finished conductor width **shall** be 0.5 mm ± 0.07 mm [0.020 in ± 0.0028 in] and finished land size **shall** be 1.8 mm ± 0.13 mm [0.0709 in ± 0.00512 in]. Hole size **shall** be consistent with process(es) being evaluated. The location of test coupons on the panel and hole diameters **shall** remain constant. The design dimensions may require compensation for process allowances.

12.4.12 Coupon X (Bending Flexibility and Endurance, Flexible Printed Wiring) This coupon is used to validate bending flexibility and bending endurance of flexible printed wiring applications. Figure 12-22 provides coupon design guidance. The final configuration of the coupon should be determined with regard for the end product application and by user/supplier agreement. The coupon X-1, X-2, X-3 (referred to within IPC-A-41 Single Sided Artwork) is typically used for product material qualification. The configuration of an X-4 style coupon is preferred for product acceptance testing of flexible products designed for installation use B (dynamic flex; See IPC-2223). The X-4 coupon should represent the circuit conductor characteristics of the actual design. The outline length of the coupon as shown in Figure 12-22 should not be deviated from in order to accommodate the test method fixture without

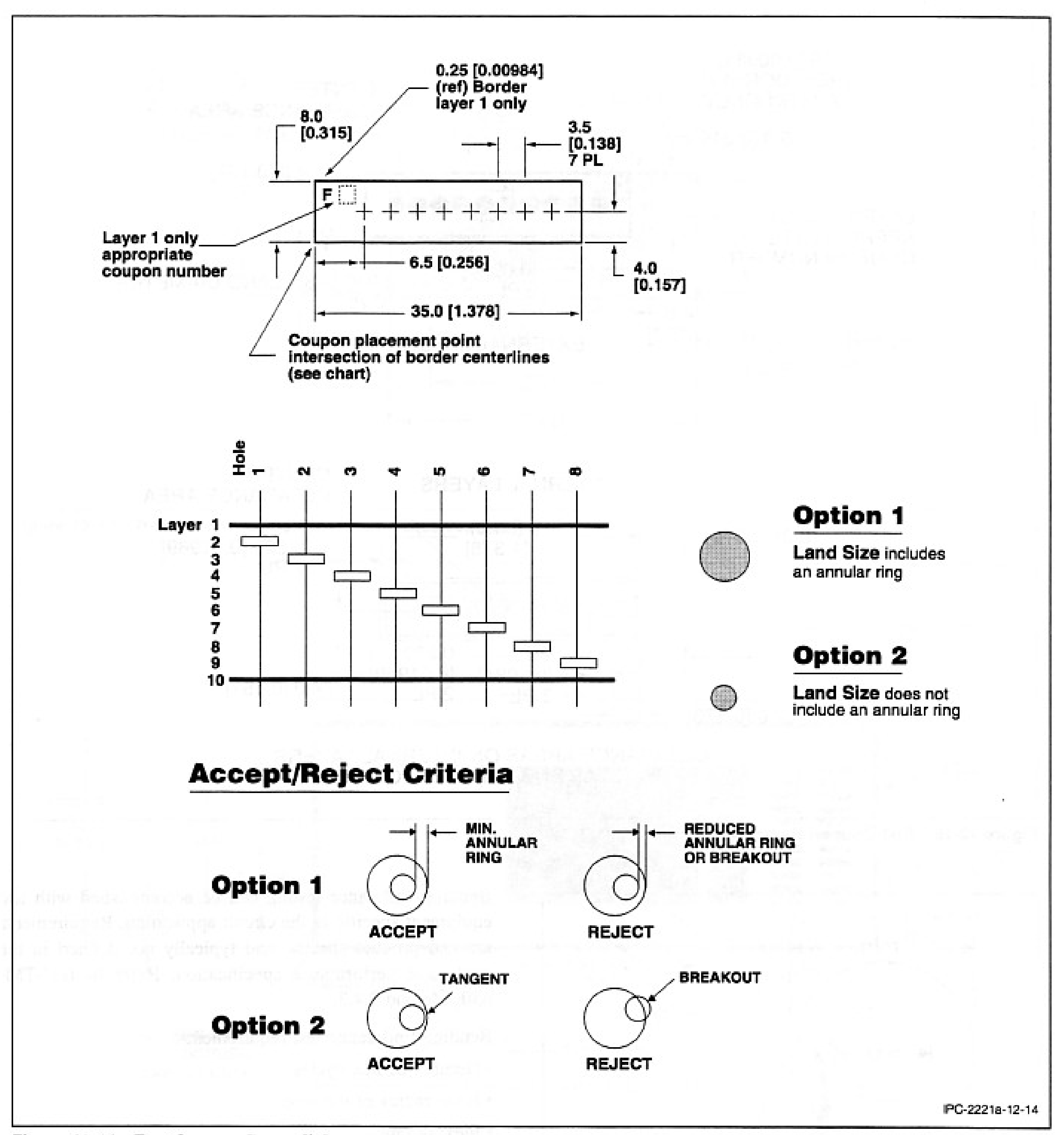


Figure 12-14 Test Coupon F, mm [in]

first consulting with the supplier. The following minimum parameters **shall** be specified on the master drawing:

Bending Flexibility test requirements; See Figure 12-23:

- Direction of bend (a)
- Degree of bend (b)
- Number of bend cycles (c)
- Diameter of mandrel (d)
- Point(s) of bend application

Note: Bend cycle is defined as taking one end of the specimen and bending it around a mandrel and then bending back to the original starting position, traveling 180° in one direction and 180° in the opposite direction. A bend cycle may also be defined as bending (using opposite ends) the ends toward each other (bend the same direction) and then bending them back to the original starting position, with each end traveling 90° in one direction and 90° in the opposite direction.

0.25 [0.00984] (REF) BORDER LAYER 1 ONLY

CENTER CLEARANCE AREA

8.0 [0.315]

35.0 [1.378]

4.0 [0.157]

LAYER 1 ONLY APPROPRIATE COUPON NUMBER

2.5 [0.0984] 9 PL

2.0 [0.0787] LAND DIAMETER 10 PL

4.0 [0.157]

EXTERNAL LAYER

INTERNAL LAYERS

CENTER CLEARANCE AREA

(8.0) [0.315]

(35.0) [1.378]

0.500 [0.01969] 2 PL

2.5 [0.0984] 8 PL

0.500 [0.01969] 2 PL

4.0 [0.157]

7.0 [0.276]

CLEARANCE AREAS ON INTERNAL LAYERS (STARTING LEFT TO RIGHT)

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Figure 12-15 Test Coupon R, mm [in]

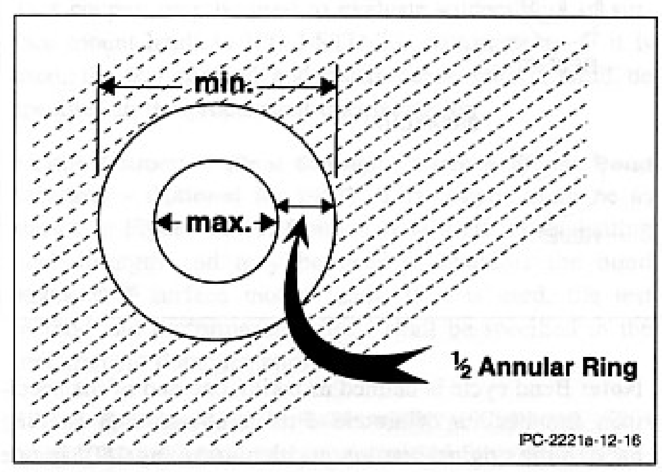


Figure 12-16 Worst-Case Hole/Land Relationship

Bending endurance testing can be accomplished with test equipment specific to the circuit application. Requirements are end product specific and typically not defined in the applicable performance specification. Refer to IPC-TM-650, Method 2.4.3.

Bending Endurance test requirements:

- Number of flex cycles
- Bend radius of the loop
- Flexing rate
- Points of application
- Travel of loop
- Method for determining end of life cycle performance (visual, electrical test, resistance change, etc.)

Refer to IPC-2223 for specific design flexibility guidelines.

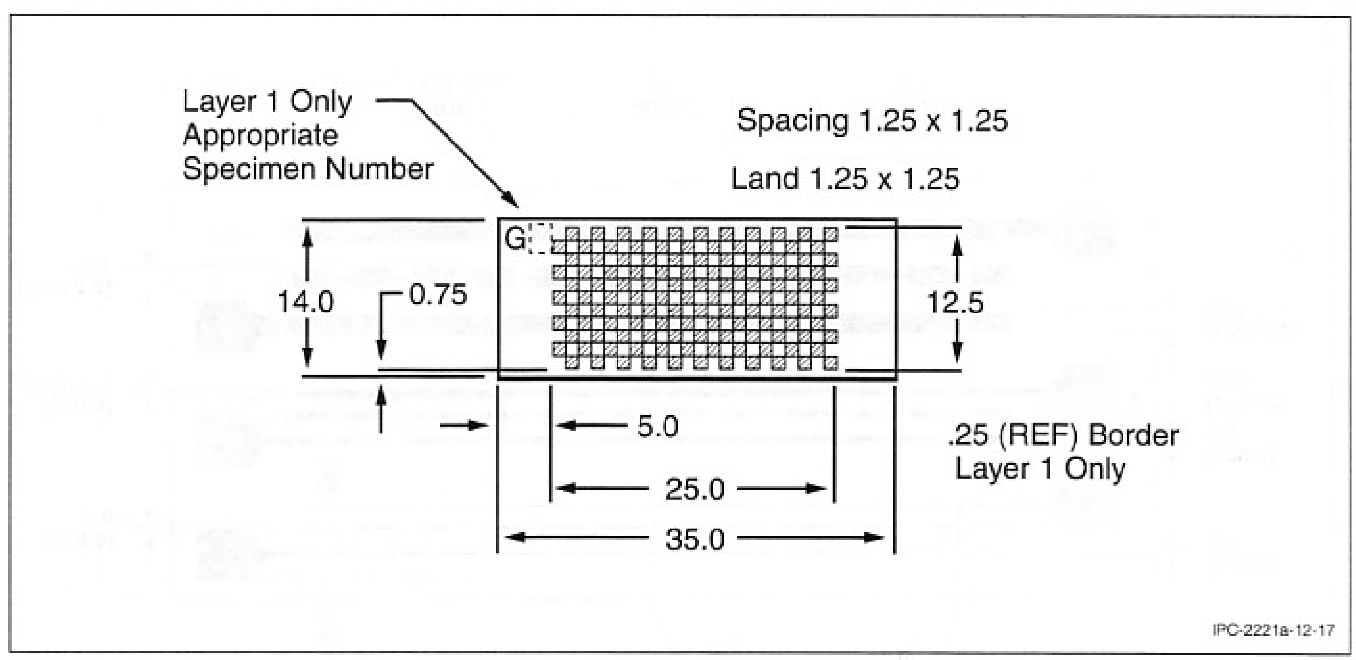


Figure 12-17 Test Coupon G, Solder Resist Adhesive, mm [in]

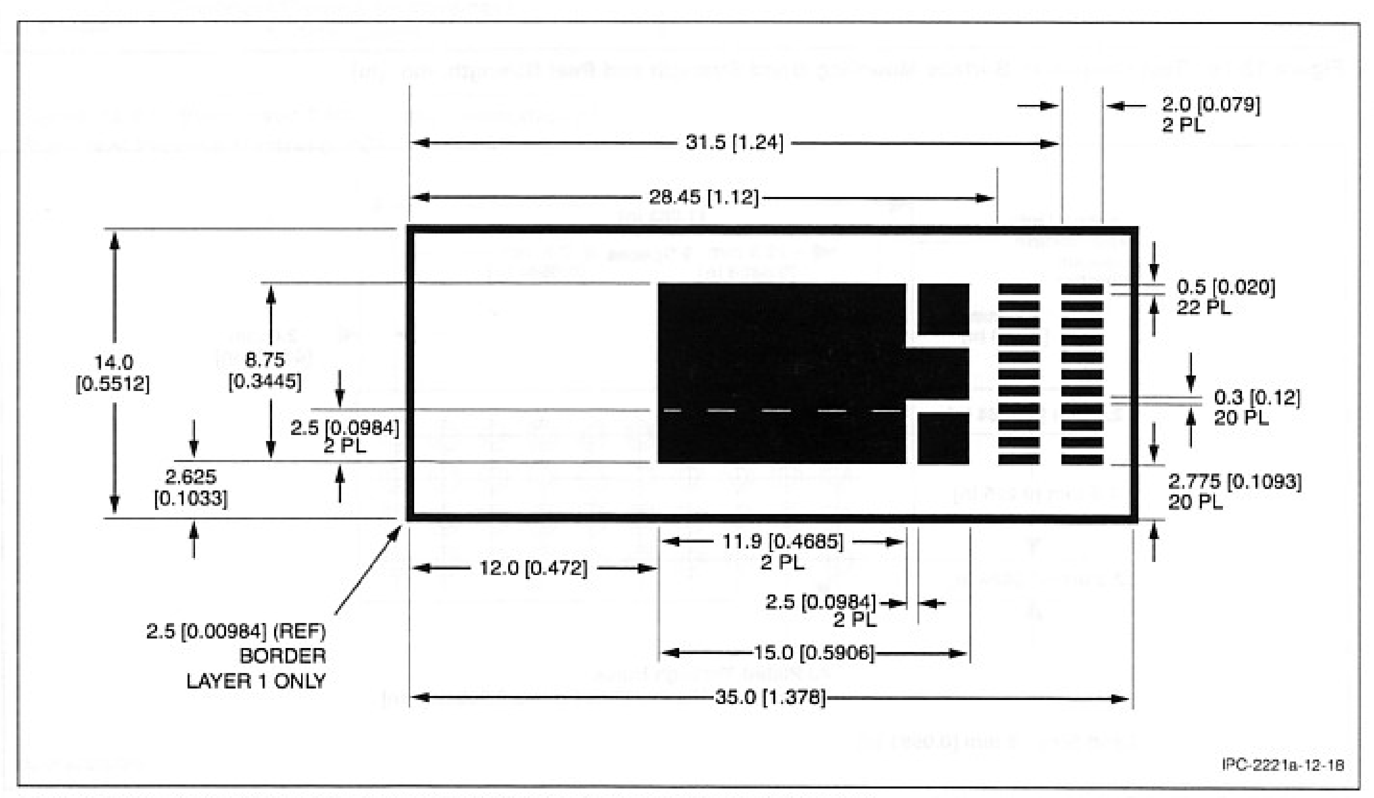


Figure 12-18 Test Coupon M, Surface Mounting Solderability Testing, mm [in]

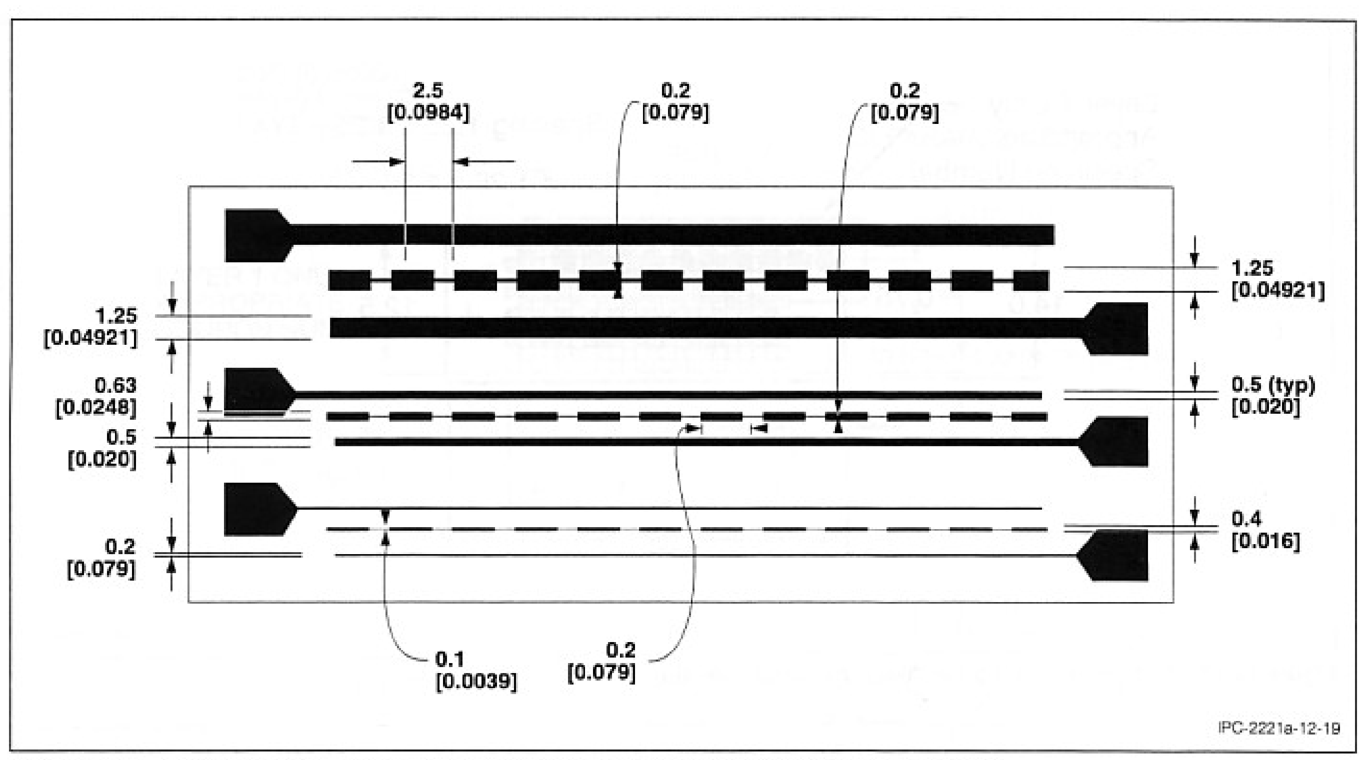


Figure 12-19 Test Coupon N, Surface Mounting Bond Strength and Peel Strength, mm [in]

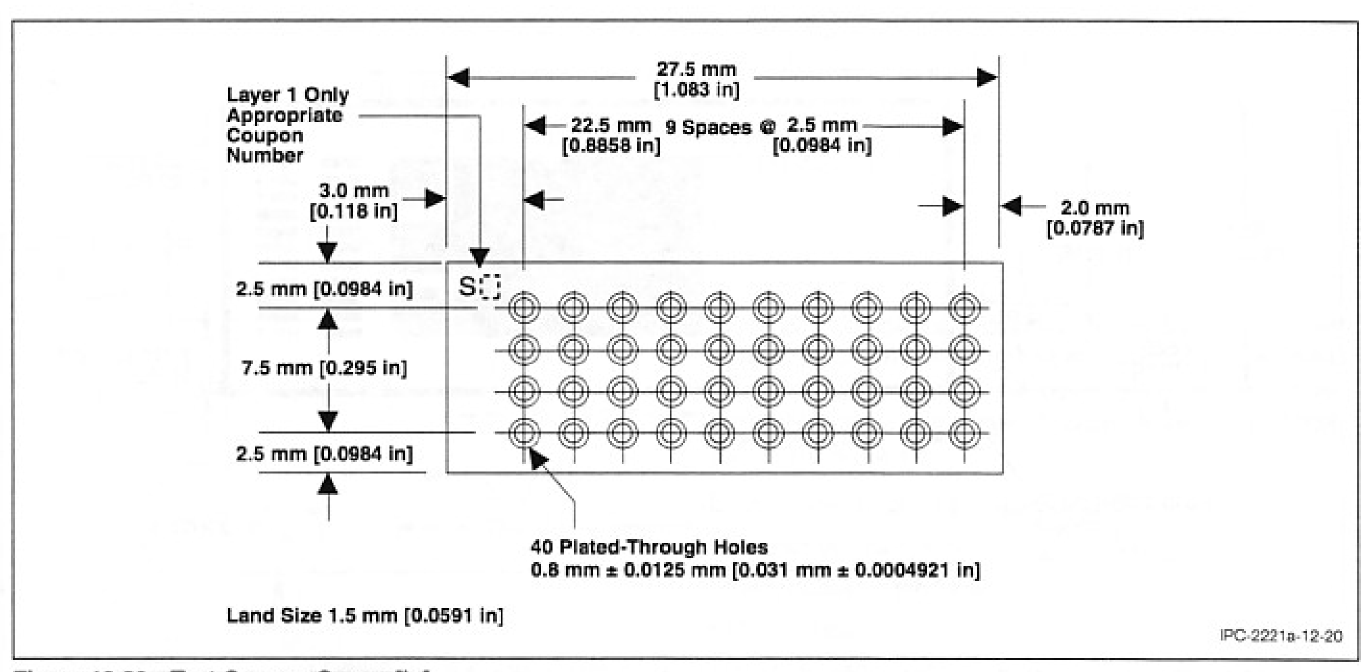


Figure 12-20 Test Coupon S, mm [in]

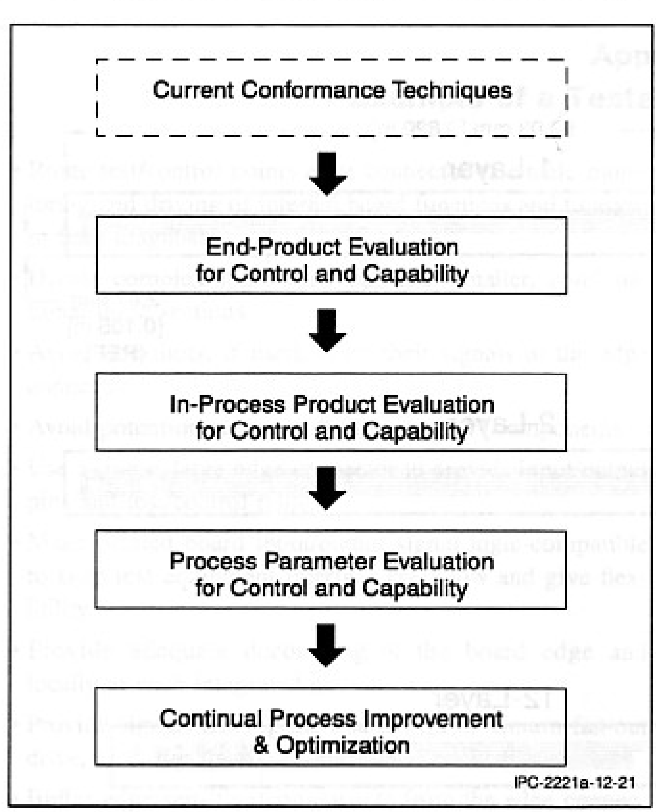


Figure 12-21 Systematic Path for Implementation of Statistical Process Control (SPC)

2.67 mm [0.105 in] (REF)

97.03 mm [3.820 in]

1-Layer

7.62 mm [0.300 in] (REF)

2.67 mm [0.105 in] (REF)

Layer Legend

1 Coupon Border
2 Common Pads
6 Drill Holes
11 Strands Layer 1
21 Strands Layer 2
31 Strands Layer 3
41 Strands Layer 4
51 Strands Layer 5
61 Strands Layer 6
71 Strands Layer 7
81 Strands Layer 8
91 Strands Layer 9
101 Strands Layer 10
111 Strands Layer 11
121 Strands Layer 12

2-Layer

2.92 mm [0.115 in] (REF)

12-Layer

2.54 mm [0.100 in] (REF)

2.04 mm [0.080 in] (REF)

50.80 mm [2.00 in]

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Figure 12-22 Test Coupon X, mm [in]

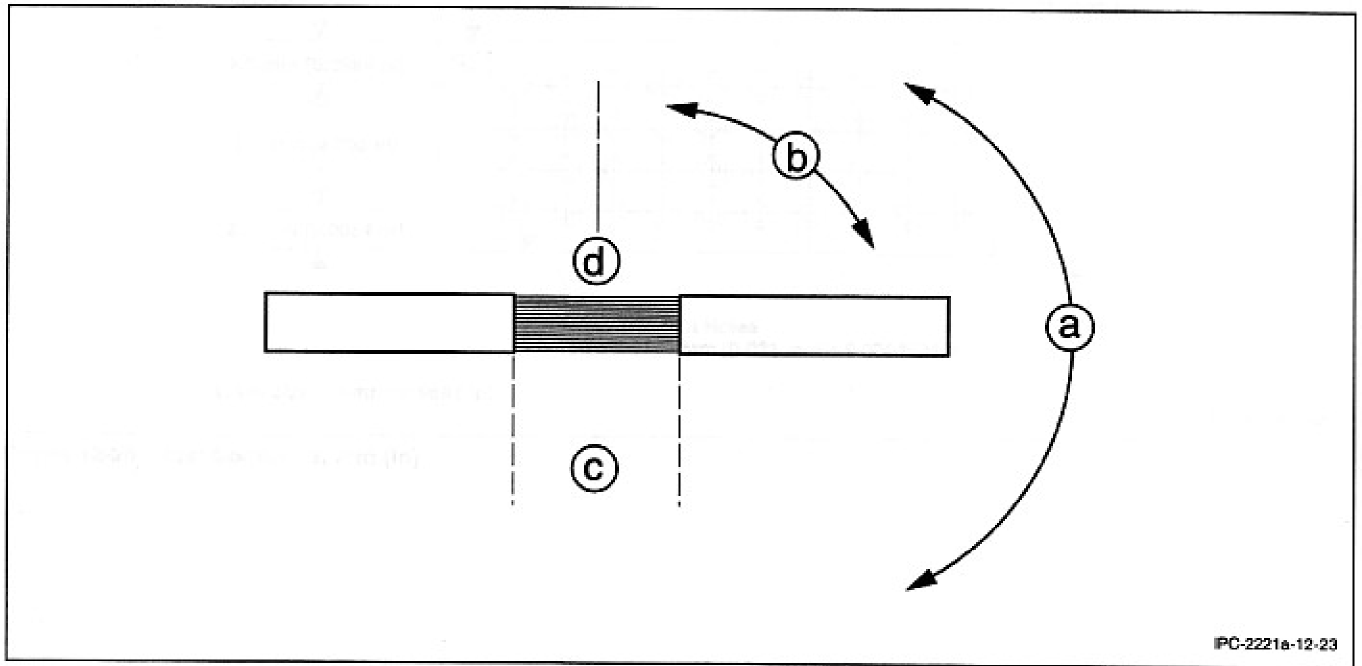


Figure 12-23 Bending Test

Appendix A
Example of a Testability Design Checklist

- Route test/control points edge connector to enable monitoring and driving of internal board functions and to assist in fault diagnosis.
- Divide complex logic functions into smaller, combinational logic sections.
- Avoid one-shots; if used, route their signals to the edge connector.
- Avoid potentiometers and "select-on-test" components.
- Use a single, large-edge connector to provide input/output pins and test/control points.
- Make printed board input/output signal logic-compatible to keep test equipment interface costs low and give flexibility.
- Provide adequate decoupling at the board edge and locally at each integrated circuit.
- Provide signals leaving the board with maximum fan-out drive, or buffer them.
- Buffer edge-sensitive components from the edge connector - such as clock lines and flip-flop outputs.
- Do not tie signal outputs together.
- Never exceed the logic rated fan-out; in fact, keep it to a minimum.
- Do not use high fan-out logic devices. Do use multiple fan-out devices, and keep their outputs separate.
- Keep logic depth on any board to a low level by using edge terminated test/control points.
- Single-load each signal entering the board whenever possible.
- Terminate unused logic pins with a resistive pull-up to minimize noise pick-up.
- Do not terminate logic outputs directly into transistor bases. Do use a series current-limiting resistor.
- Buffer flip-flop output signals before they leave the board.
- Use open-collector devices with pull-up resistors to enable external override control.
- Avoid using redundant logic to minimize undetectable faults.
- Bring outputs of cascaded counters to higher-order counters so that they can be tested without large counts.
- Construct trees to check the parity of selected groups of eight bits or fewer.
- Avoid "wired'OR" and "wired'AND" connections. If you cannot, use gates from the same integrated circuit package.
- Provide some way to bypass level-changing diodes in series with logic outputs.
- Break paths when a logic element fans out to several places that converge later.
- Use elements in the same integrated circuit package when designing a series of inverters or inverters following a gate function.
- Standardize power-on and ground pins to avoid test-harness multiplicity.
- Bring out test points as near to digital-to-analog conversion as possible.
- Provide a means of disabling on-board clocks so that the tester clock may be substituted.
- Provide mounted switches and resistor-capacitor networks with override lines to the edge-board connector.
- Route logic drivers of lamps and displays to the edge connector so that the tester can check for correct operation.
- Divide large printed boards into subsections whenever possible, preferably by function.
- Separate analog circuits from digital logic, except for timing circuits.
- Uniformly mount integrated circuits and clearly identify them to make it easier to locate them.
- Provide sufficient clearance around integrated circuit sockets and direct-soldered integrated circuits so that clips can be attached whenever necessary.
- Add top-hat connector pins or mount extra integrated circuit sockets when there are not enough edge-board connector pins for test/control points.
- Use sockets with complex integrated circuits and long, dynamic shift registers.
- Wire feedback lines and other complex circuit lines to an integrated circuit package.
- Use jumpers that can be cut during debugging. The jumpers can be located near the edge-board connector.
- Fix locations of power and ground lines for uniformity among several board types.
- Make the ground conductor large enough to avoid noise problems.
- Group together signal lines of particular families.
- Clearly label all parts, pins and connectors.

Appendix B
Conductor Current-Carrying Capacity and Conductor Thermal Management

1 Purpose

An update of the conductor current-carrying capacity charts is in progress as of the release of Revision A to the IPC-2221. This appendix is included as a discussion and clarification of the existing charts. It is also intended as a notice to the industry that new design guidelines are being prepared and that training will be available to maximize the use of the new information. The forthcoming standard will be IPC-2152, *Standard for Determining Current-carrying Capacity in Printed Board Design.*

The existing charts are, for the most part, conservative. In this context conservative means that more current can be applied to the conductor for the intended temperature rise. The IPC-2152 will provide a better understanding of the conductor temperature response. This is necessary to meet the demands of the existing trends occurring in the electronics industry.

2 Original Design Guide

A National Bureau of Standards (NBS) progress report, No. 4283, titled *"Characterization of Metal-Insulator Laminates"*, by D. S. Hoynes, dated May 1, 1956, was published for the Navy Bureau of Ships. The report discussed progress on a project that was established for the purpose of determining physical and electrical properties suitable for the evaluation of metal-insulator laminates for use in printed circuit applications. This report was a continuation of the work described in NBS Report No. 3392, *"Characterization of Metal-Insulator Laminates,"* dated June 30, 1954. NBS 3392 did not pertain to current-carrying capacity.

NBS Report No. 4283 dealt with tests conducted on the current-carrying capacity of etched copper conductors, resistance measurements on samples having a variety of protective coatings, and dielectric properties of a number of metal-clad laminates at various temperatures.

A chart showing the relationship between temperature rise, conductor width, cross-sectional area, and copper thickness was developed as a design aid for determining conductor sizes in printed circuit application utilizing etched conductors and is shown in Figure B-1. This is the same chart that is used today for external conductors.

This design chart was assembled for use primarily with phenolic (XXXP) and Epoxy-glass materials of 1/16 (0.0625 inch) to 1/8 (0.125 inch) inch thickness and copper thickness of 0.00135 inch (1 ounce) and 0.0027 inch (2 ounce). Table B-1 lists a short description of each of the

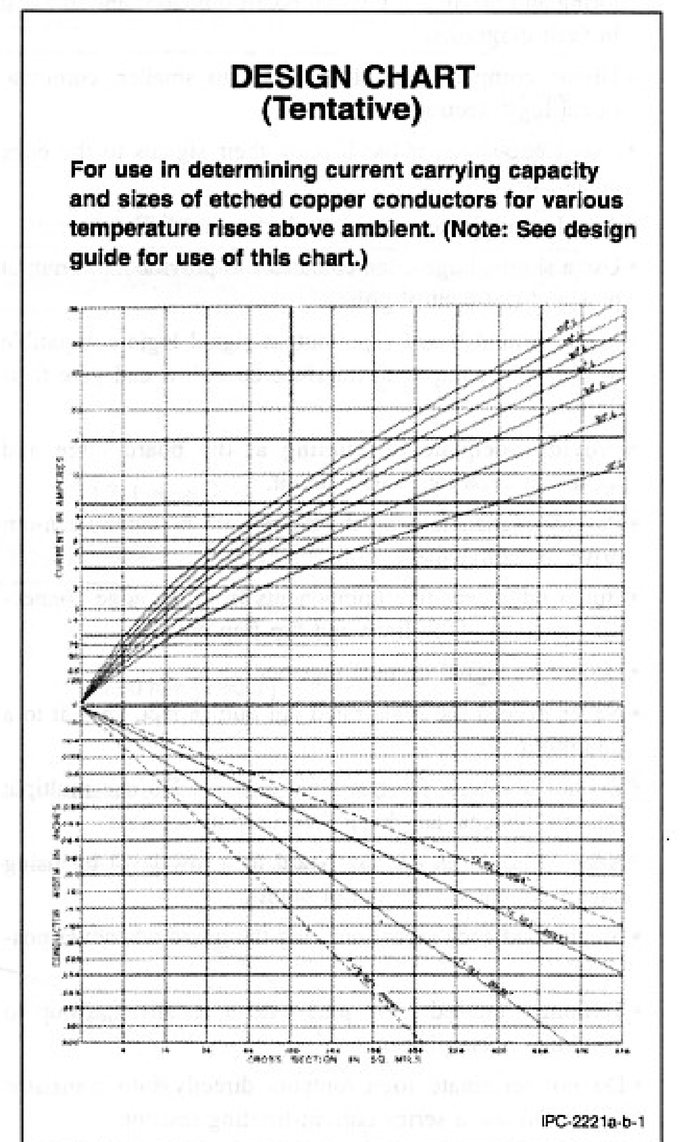


Figure B-1 Original Design Chart

test boards used to create the chart in Figure B-1. This chart, shown here as Figure B-2, was then adopted for use in the military standards, which led to the IPC-2221A external charts within Figure 6-4 of the design standard.

3 Internal Conductors

Testing was not performed to evaluate internal conductor current-carrying capacity. The internal conductor charts are based on half of the current from the external conductor chart, Figure B-1. Acknowledgement of this and the desire for more flexibility for sizing electrical conductors led to the creation of the IPC 1-10b Current Carrying Capacity Task Group.

Table B-1 Test Samples

Code	Material and Core Thickness (in.)	Copper Thickness (in)[1]	Additional Processing	Test Temp (°C)	Test Method[2]
A	5-7 XXXP 1/16	0.0027 KK	None	50	IR & TC
B	2-7 XXXP 1/16	0.004 K	None	50	IR & TC
C	4-7 XXXP 1/16	0.00135 K	None	50	IR
D	4-10 Epoxy 1/16	0.00135 K	None	50	IR & TC
E	5-7 XXXP 1/16	0.0027 K	None	60	IR & TC
F	2-7 XXXP 1/16	0.0027 K	None	60	IR
G	4-7 XXXP 1/16	0.00135 KK	None	60	IR
H	5-7 XXXP 1/16	0.0027 KK	None	25	IR
I	2-7 XXXP 1/16	0.004 K	None	25	IR & TC
J	5-10 Epoxy 1/16	0.0027 K	None	25	IR
K	4-7 XXXP 1/16	0.00135 KK	None	25	IR
L	5-10 Epoxy 1/32	0.00135 K	None	25	IR
M	4-10 Epoxy 1/16	0.00135 K	None	25	TC
N	2-7 XXXP 1/16	0.00067 K	None	25	IR
O	5-10 Epoxy 1/32	0.00135 KK	None	25	IR
P	4-10 Epoxy 1/16	0.00135 K	Coated with 0.005″ epoxy resin	25	IR
Q	2-7 XXXP 1/16	0.00135 K	Coated with 0.002″ insulating varnish	25	IR
R	5-7 XXXP 1/16	0.0027 K	Coated with 0.001″ silicone spray	25	IR
S	4-7 XXXP 1/16	0.00135 K	Coated with 0.003″ insulating varnish	25	IR
T	2-7 XXXP 1/16	0.0027 K	Coated with 0.006″ silicone resin	25	IR
U	2-7 XXXP 1/16	0.00135 K	Dip soldered 10 sec 250 °C	25	IR
V	2-7 XXXP 1/16	0.0027 K	Dip soldered 10 sec 250 °C	25	IR
W	10-7 XXXP 1/16	0.00135 K	Dip soldered 10 sec 250 °C	25	IR
X	5-10 Epoxy 1/8	0.0027 K	Dip soldered and coated with 0.005 epoxy resin	25	IR & TC
Y	4-7 XXXP 1/16	0.00135 K	Dip soldered 10 sec 250 °C	25	IR
Z	2-7 XXXP 1/16	0.0027 K	Dip soldered 10 sec 250 °C	25	TC
1	5-7 XXXP	0.00135	Core removed conductor in free air (CRFAIR)	25	IR
2	6-16 G-5	0.00135	(CRFAIR)	25	IR
3	2-7 XXXP	0.00135	(CRFAIR)	25	IR
4	5-7 XXXP	0.0027	(CRFAIR)	25	IR
5	2-7 XXXP	0.0027	(CRFAIR)	25	IR
6	2-7 XXXP	0.0027	(CRFAIR)	25	IR
7	4-10 Epoxy	0.00135	(CRFAIR)	25	IR

1. K denotes single clad and KK denotes double clad.
2. IR = Resistance Change Measurement, TC = Thermocouple Measurement.

4 IPC 1-10b Current Carrying Capacity Task Group

The IPC 1-10b Current Carrying Capacity Task Group is developing the IPC-2152 for conductor current-carrying capacity. This group is investigating the variables that affect the temperature of a conductor when an electrical current is applied. The primary focus is on internal conductors and the group has results from testing and thermal modeling. The variables that are under investigation are conductor width and thickness, board material and thickness, internal copper planes, environment (air, vacuum), time dependencies and power dissipation. A training program will be instituted along with the IPC-2152 to educate users with the use of the new standard.

Some of the task group's results are included in Figures B-3 through B-5. A single trace was arbitrarily selected to compare against the values in the internal conductor-sizing chart. The results shown in these figures are all for internal conductors. Figure B-3 shows how board thickness affects a conductor temperature.

(For use in determining current carrying capacity and sizes of etched copper conductors for various temperature rises above ambient.)

CURRENT IN AMPERES

CROSS SECTION IN SQ. MILS

Figure A External Conductors

CONDUCTOR WIDTH IN INCHES

CROSS SECTION IN SQ. MILS

Figure B Conductor width to cross-section relationship

IPC-2221a-b-2

Figure B-2 IPC 2221A External Conductor Chart

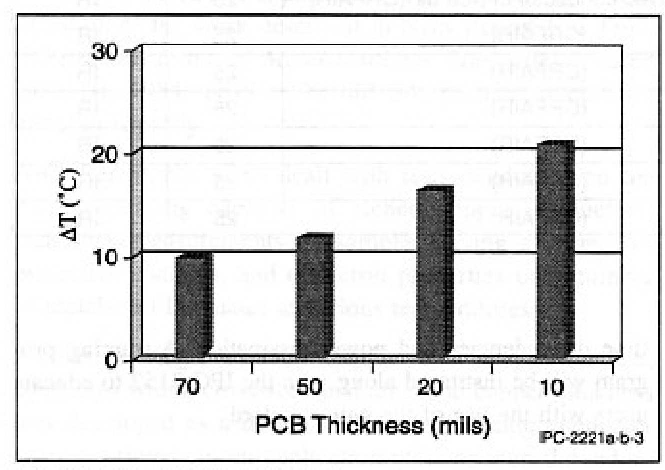


Figure B-3 Board Thickness

Figure B-4 helps to illustrate the disparity between the existing internal conductor charts and results from the task group studies. The current is applied to the same size trace in each board configuration. The only difference in all cases is the board material thermal properties. The IPC delta T, or ΔT, is determined using equations that represent the IPC internal conductor charts. This shows the conservative nature of using half the current from the external conductor chart. Phenolic, known as XXXP, is included since this is the material that was primarily used to create the existing charts.

Figure B-5 shows results from air and vacuum testing. This helped quantify how much higher the conductor temperatures run in vacuum than in air. Enough of a difference exists to warrant a section on various environmental conditions.

5 Thermal Management Sizing electrical conductors is going to be a thermal management topic. Designs will have the flexibility to size conductors smaller or larger based on the thermal requirements of the specific design. This flexibility in the design will be possible through the use of a new methodology for conductor sizing. The methodology will be introduced in the new standard.

6 Publication of the New Standard The first draft of the IPC-2152 is projected for review in the first quarter of 2003.

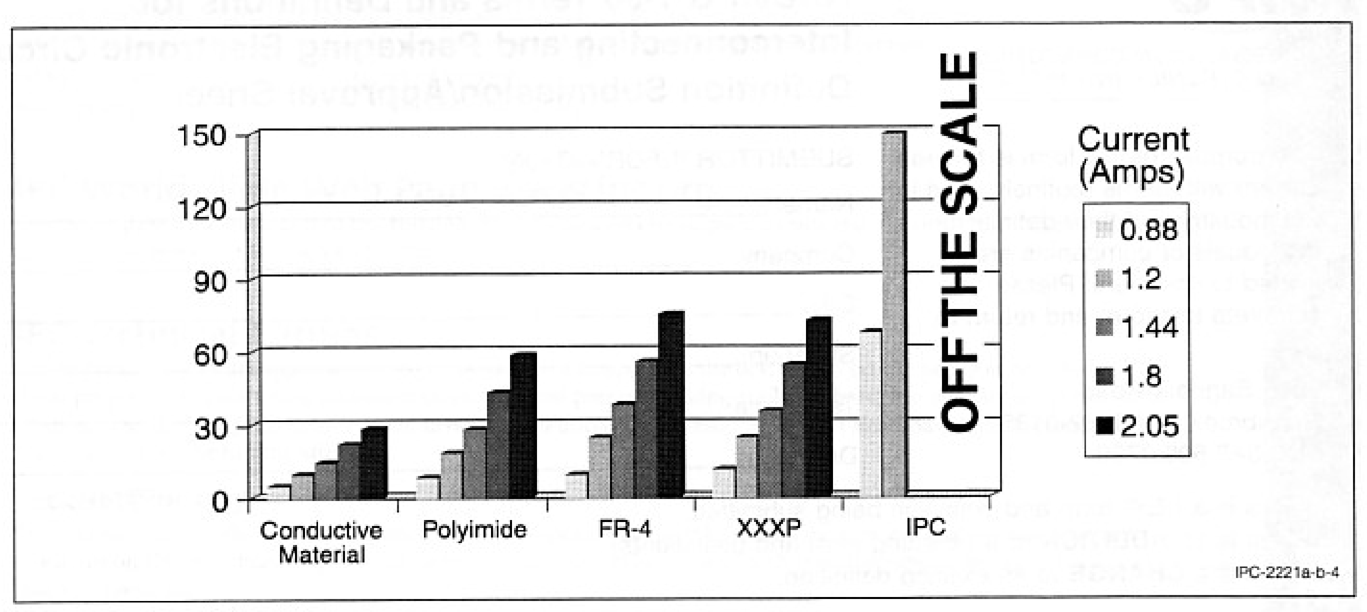


Figure B-4 Board Material

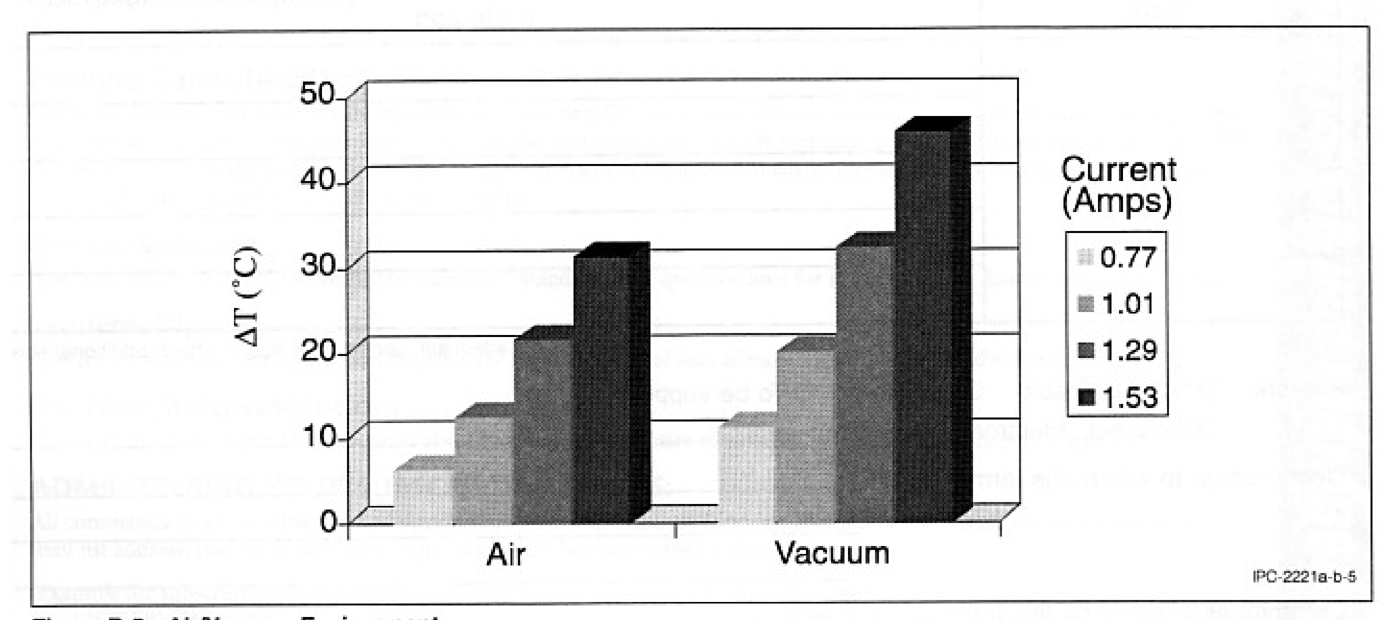


Figure B-5 Air/Vacuum Environment



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Message: signoff DesignerCouncil

Please note you must send messages to the mail list address ONLY from the e-mail address to which you want to apply changes. In other words, if you want to sign off the mail list, you must send the signoff command from the address that you want removed from the mail list. Many participants find it helpful to signoff a list when travelling or on vacation and to resubscribe when back in the office.

How to post to a forum:

To send a message to all the people currently subscribed to the list, just send to <mail list>@ipc.org. Please note, use the mail list address that you want to reach in place of the <mail list> string in the above instructions.

Example:
To: TechNet@IPC.ORG
Subject: <your subject>
Message: <your message>

The associated e-mail message text will be distributed to everyone on the list, including the sender. Further information on how to access previous messages sent to the forums will be provided upon subscribing.

For more information, contact Keach Sasamori
tel 847/790-5315 fax 847/504-2315
e-mail: sasako@ipc.org www.ipc.org/html/forum.htm

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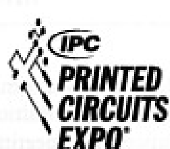
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For information on how to get involved, contact:
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